Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes

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Department of Electrical Engineering

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Declaration

I declare that this written submission represents my idea in my own words, and where others' ideas and words have been included, I have adequately cited and the reference the original sources. I also declare that I have adhered to all principles of academic history and integrity and have not misrepresented or fabricated or falsified any idea /data /fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can evoke panel action from the sources that have thus not been properly cited, or from whom proper permission has not been taken when needed.

Ashok Kumar Singh

ASHOK KUMAR SINGH

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Approval Sheet

This thesis **Capacitance to Digital Converter for Ultra low power Wireless Sensor node** by **Ashok Kumar Singh** is approved for the degree of Master of Technology from IIT Hyderabad.

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ABSTRACT

Power consumption is one of the main design constraints in today's integrated circuits. For systems like wearable electronics, UAVs, IOT systems powered by batteries which are charged using the energy harvested from various sources like RF, Thermal, Solar and Vibration, ultra-low power consumption is paramount. In these systems, Transducers which convert physical parameters into electrical parameters and the analog-to-digital converters (ADCs) are key components as the interface between the analog world and the digital domain. This thesis addresses the design challenges, strategies, as well as circuit techniques of ultra-low-power signal Front End used in several low power electronic systems in general and pressure measurement systems in particular.

In this thesis, Capacitance to Digital Converter based pressure measurement system has been implemented. Here we present a general-purpose, wide-range CDC that combines a correlated double sampling (CDS) approach with a differential asynchronous SAR ADC. Since the sensor capacitor is sampled only twice per conversion, energy per conversion is low. Furthermore, since the CDS separates the sensor capacitor from the CDAC, a full differential input voltage range is preserved. The CDC has a 2.5-to-75.5pF conversion range. Monotonic SAR ADC was designed in 180nm CMOS with 1-V power supply and a 1-kS/s sampling rate with switching energy of about 100nW.

Nomenclature

CDS	Correlated double sampling
Cref	Reference Capacitor
Csens	Sensor Capacitor
Csampling	Sampling Capacitor
ADC	Analog to Digital Converter
BWC	Binary-Weighted Capacitor
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
DFF	D Flip Flop
DFT	Discrete Fourier Transform
DNL	Differential Non Linearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
FOM	Figure of Merit
IC	Integrated Chip
INL	Integral Non Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	N Type CMOS Transistor
PMOS	P Type CMOS Transistor
SAR	Successive Approximation Register
SINAD	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
S/H	Sample and Hold

Contents

Chapter 1

INTRODUCTION

1.1 Motivation

Sensors that are printed on flexible substrates called flexible sensors are going to be the next generation breakthrough in the field of environmental sensing in various areas as shown in Fig.1. They are mostly Self Powered and Stand Alone systems that find a place in modern SoC and IoT systems. Flexible electronics find their use in plenty of applications such as bio-medical, smart cities, aerospace etc. as shown in Fig 1. These wireless systems are generally powered by batteries and hence their lifetime is limited. Multi-Source energy harvesting to power these devices is an effective technique due to low area, component count and cost. Also the use of low power smart architecture for effective utilization of available power leads to extremely meagre and frugal battery usage.

1.1.1 Bio-Medical –

Flexible electronics are the next generation of sensors for mobile health and implantation. Some of them include artificial pacemaker, cochlear implant.

1.1.2 Smart Cities -

(a)Structural Health Monitoring (Smart Building), (b) Vehicle Auto-Diagnosis (Smart Transportation) - Information collection from CAN Bus to send real time indications in case of emergencies or provide alarm to drivers. Different sensors in the car can be powered by exploiting all the renewable sources available inside car.

1.1.3 Aerospace–

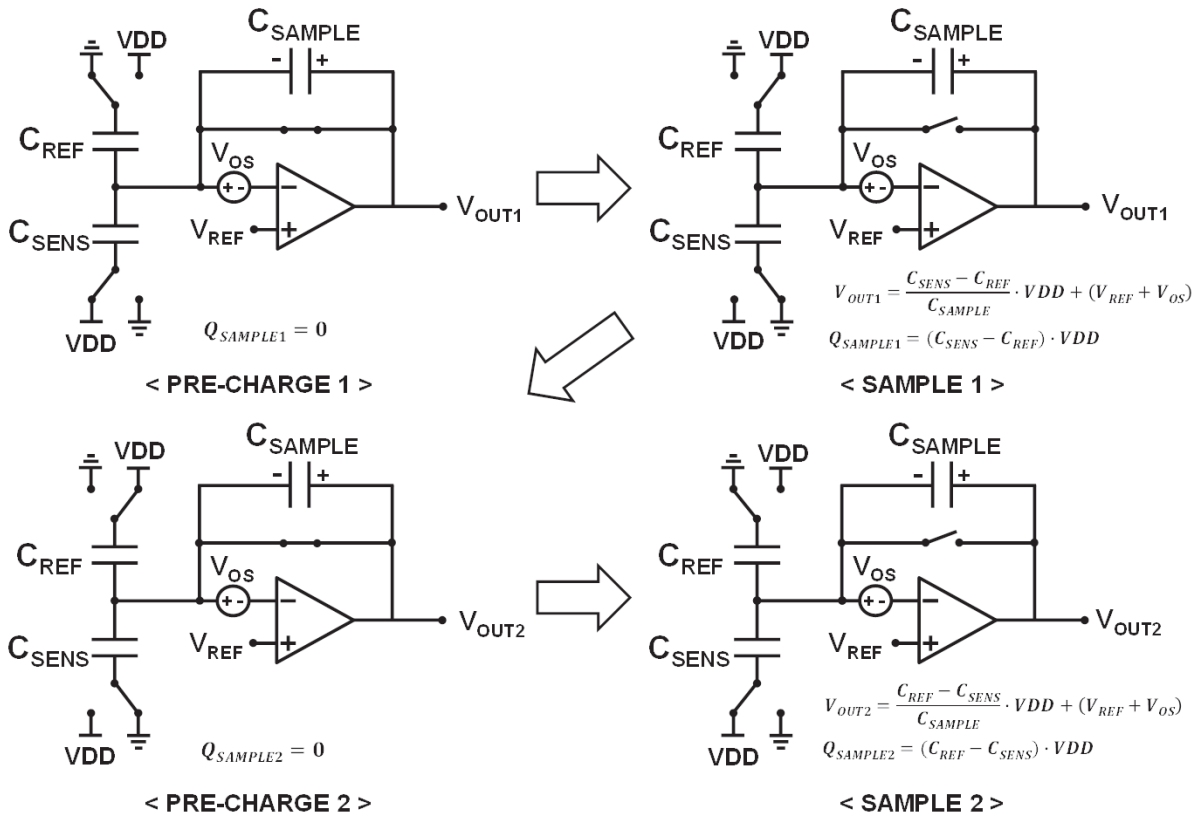
In miniature UAVs the size and power consumption of the device is the utmost priority. It requires the flexible sensor and the low power electronics with energy harvesting module

Figure 1 Applications of Flexible sensors and Low Power Electronics

1.2 Capacitor

Recent advances in nW-level wireless sensor nodes have created opportunities in emerging applications such as bio-implantable telemetry, smart healthcare, and environmental monitoring. At the same time, there are many circuit and system design challenges to achieving high functionality in such ultra-low-power microsystems. One of the key sensing modalities in these systems is capacitive sensing. With zero static current during signal readout, capacitive sensing is well suited to ultra-low-power microsystems and has been widely adopted in the sensing of pressure. This thesis presents how capacitor is used as a sensing element for pressure measurement in detail in the following chapters.

1.3 Full System Architecture and Timing Diagram of Correlated Double Sampling Technique.



$$V_{OUT} = V_{OUT1} - V_{OUT2} = 2 \cdot \frac{C_{SENS} - C_{REF}}{C_{SAMPLE}} \cdot VDD$$

$$Q_{SAMPLE} = Q_{SAMPLE1} - Q_{SAMPLE2} = 2 \cdot (C_{SENS} - C_{REF}) \cdot VDD$$

Figure : The concept of the readout frontend with correlated double sampling.

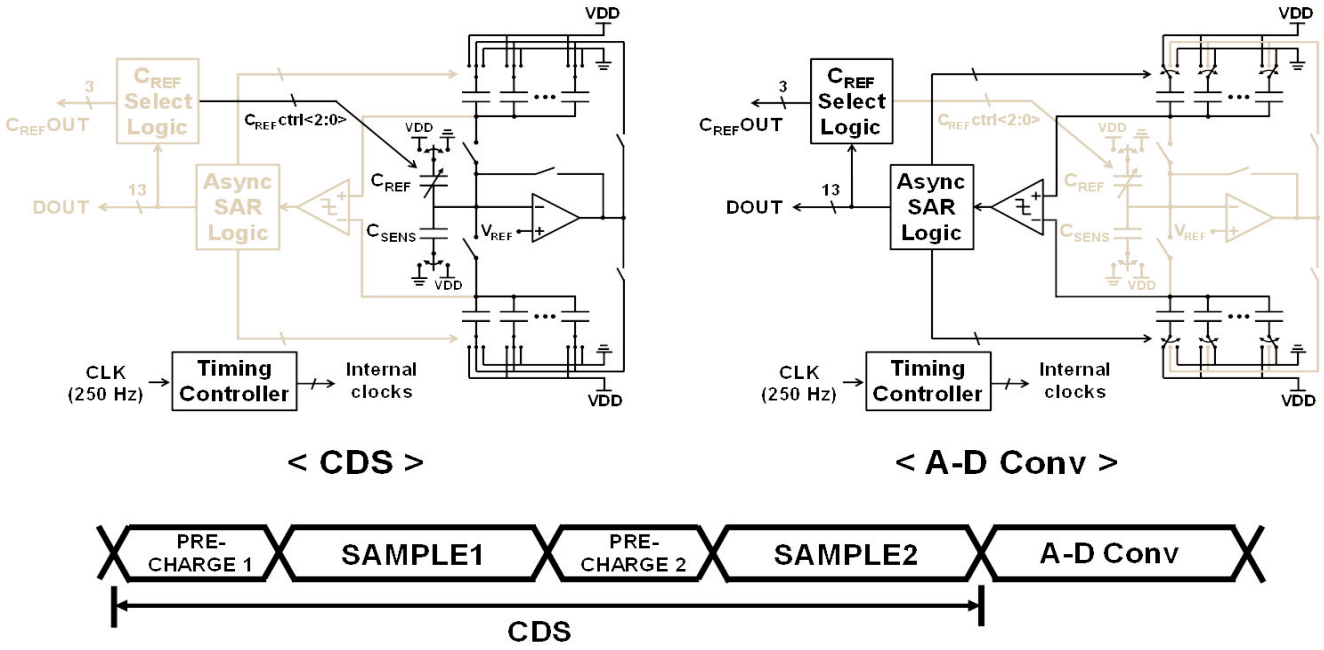
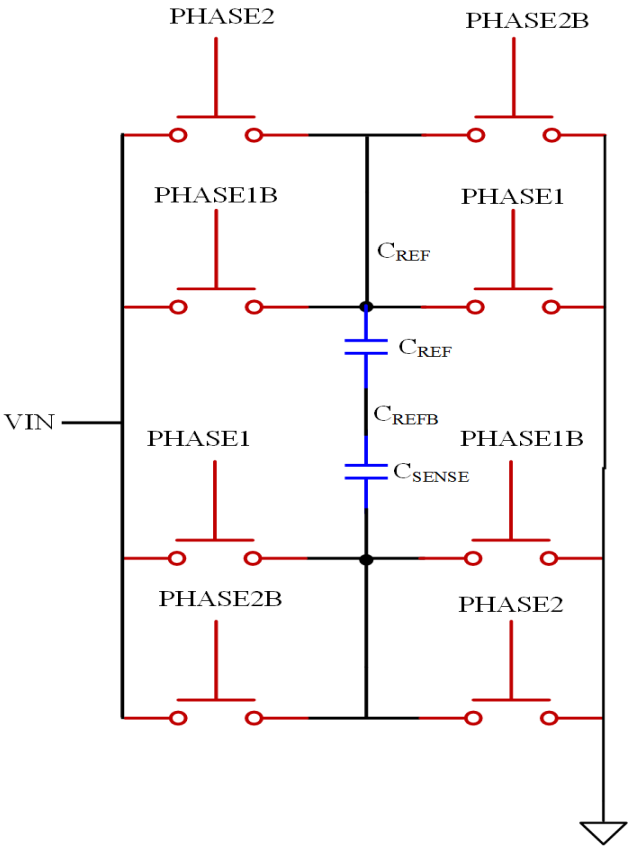


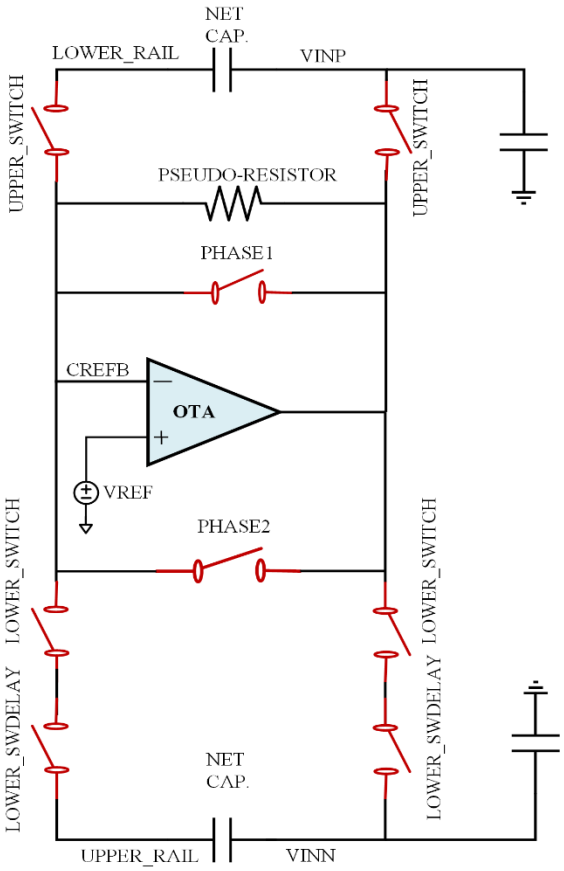
Figure: Circuit and timing diagram of the CDC.

1.4 Front End Architecture of the Pressure Sensor

Literature suggests that there are many Front Ends of measuring pressure, using capacitors, which have been successfully implemented differently for different purposes. Brief description of my work is presented here.

1.4.1 AFE for Pressure Sensor





1.4.2 Automatic Control Logic for AFE

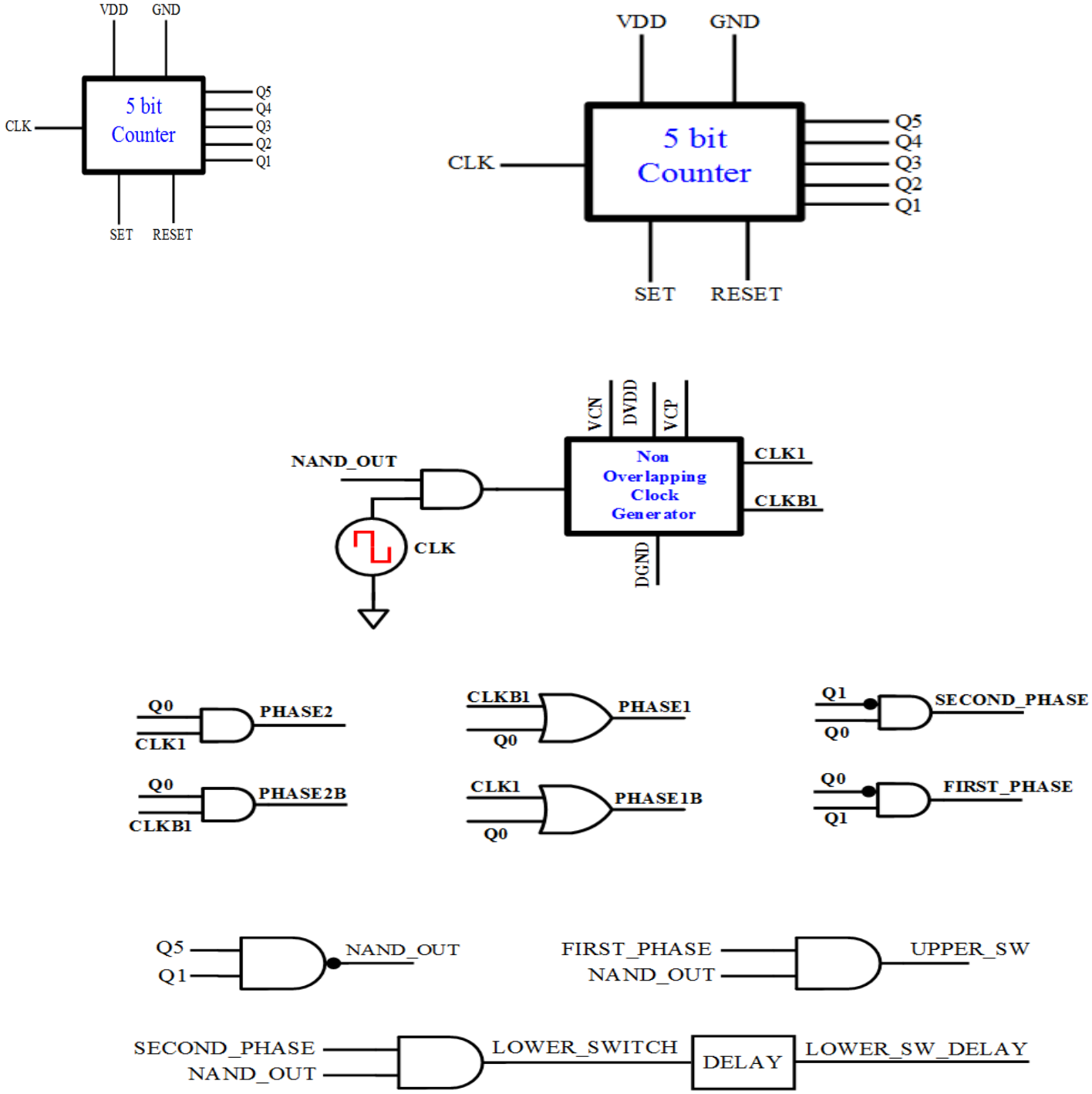


Figure 2

1.4.3 Timing Diagram for AFE

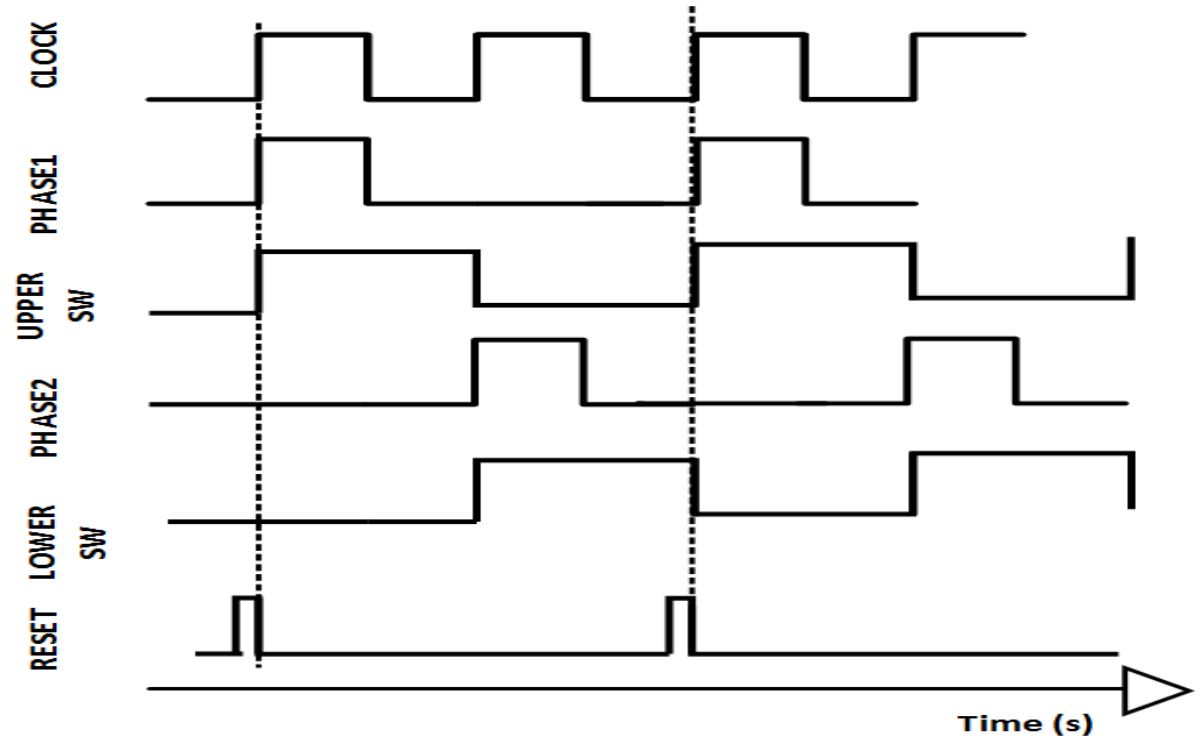


Figure 3

1.4.4 C_{REF} Select Logic

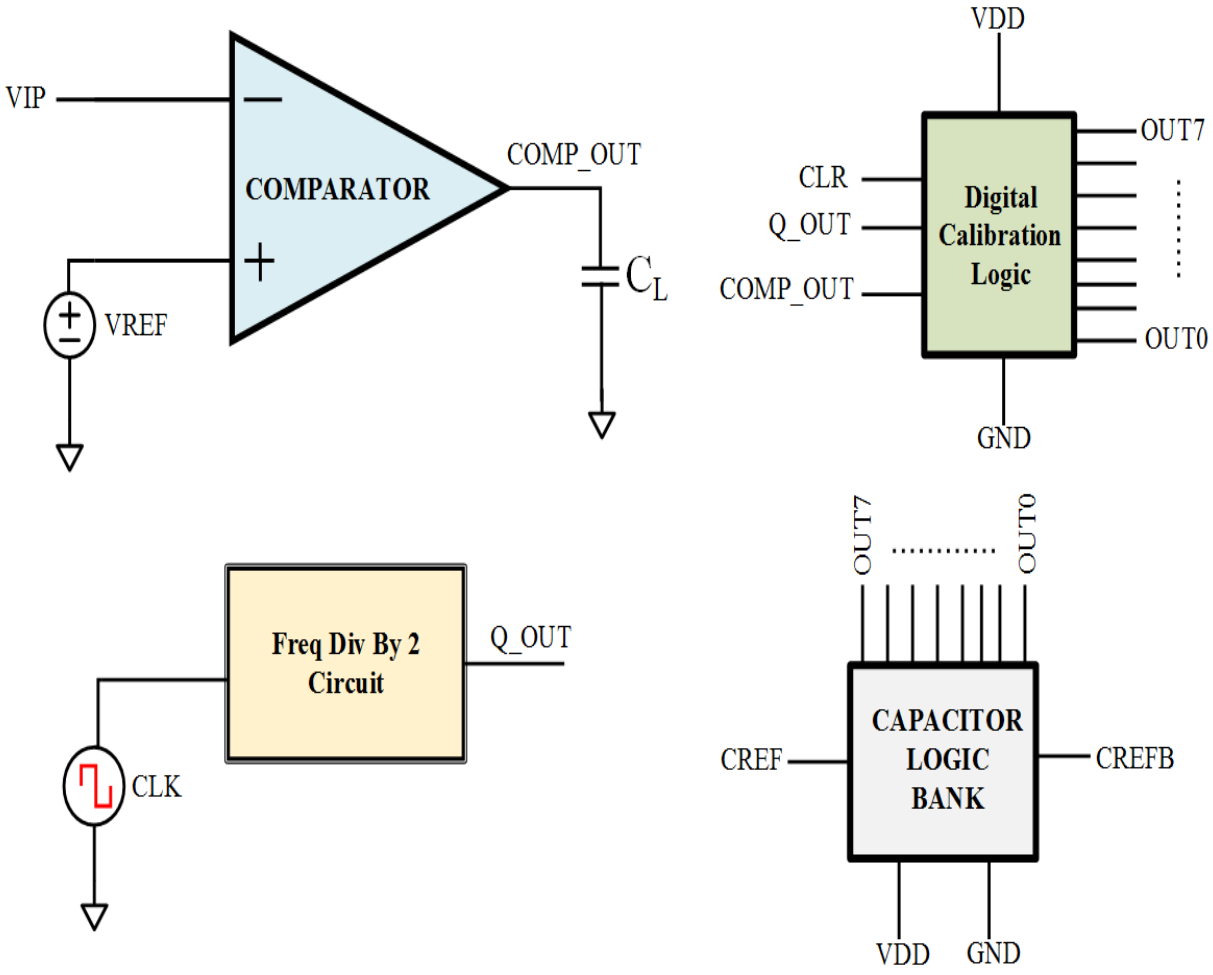


Figure 4

1.4.5 Timing Diagram for C_{REF} Select Logic

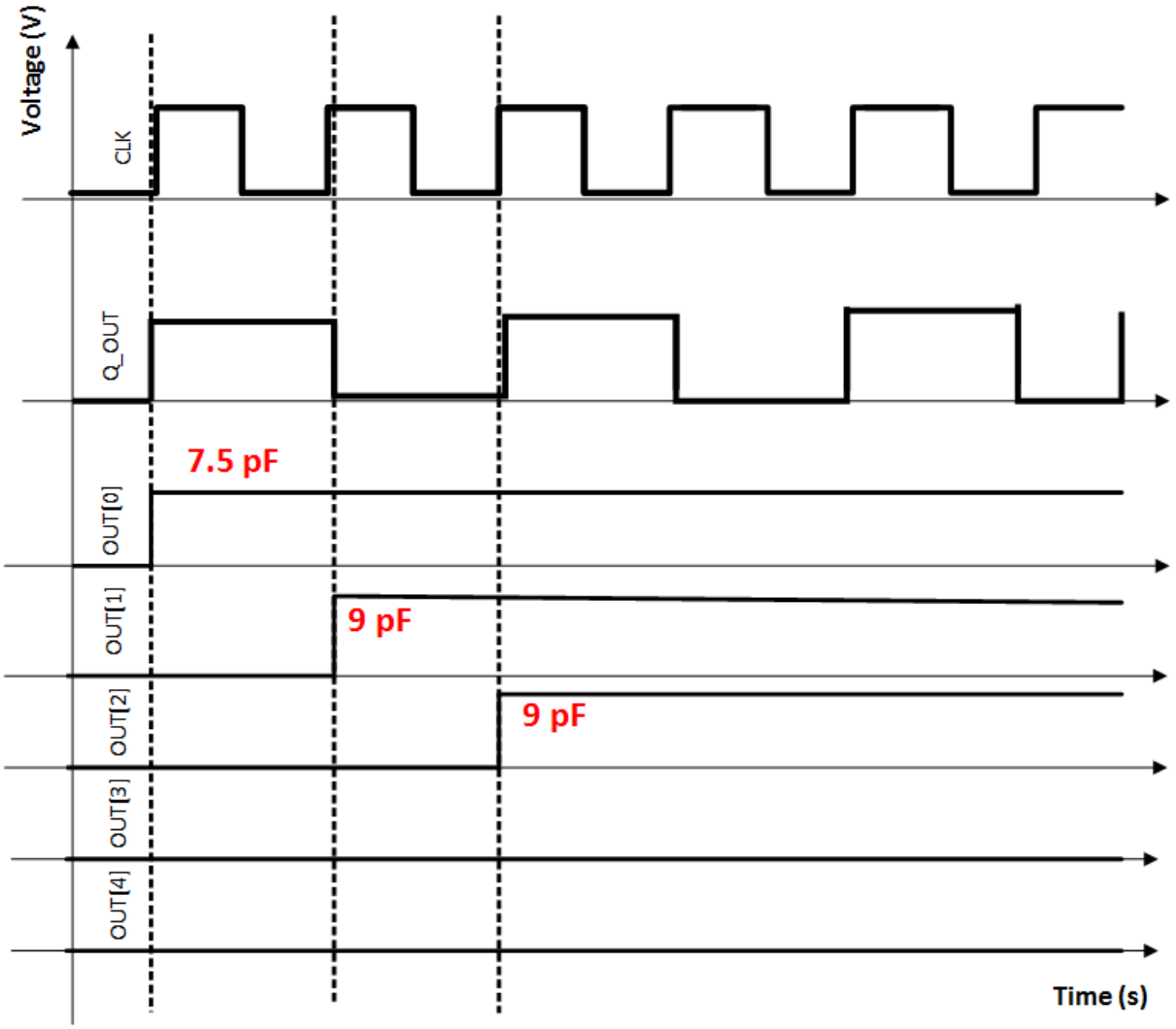
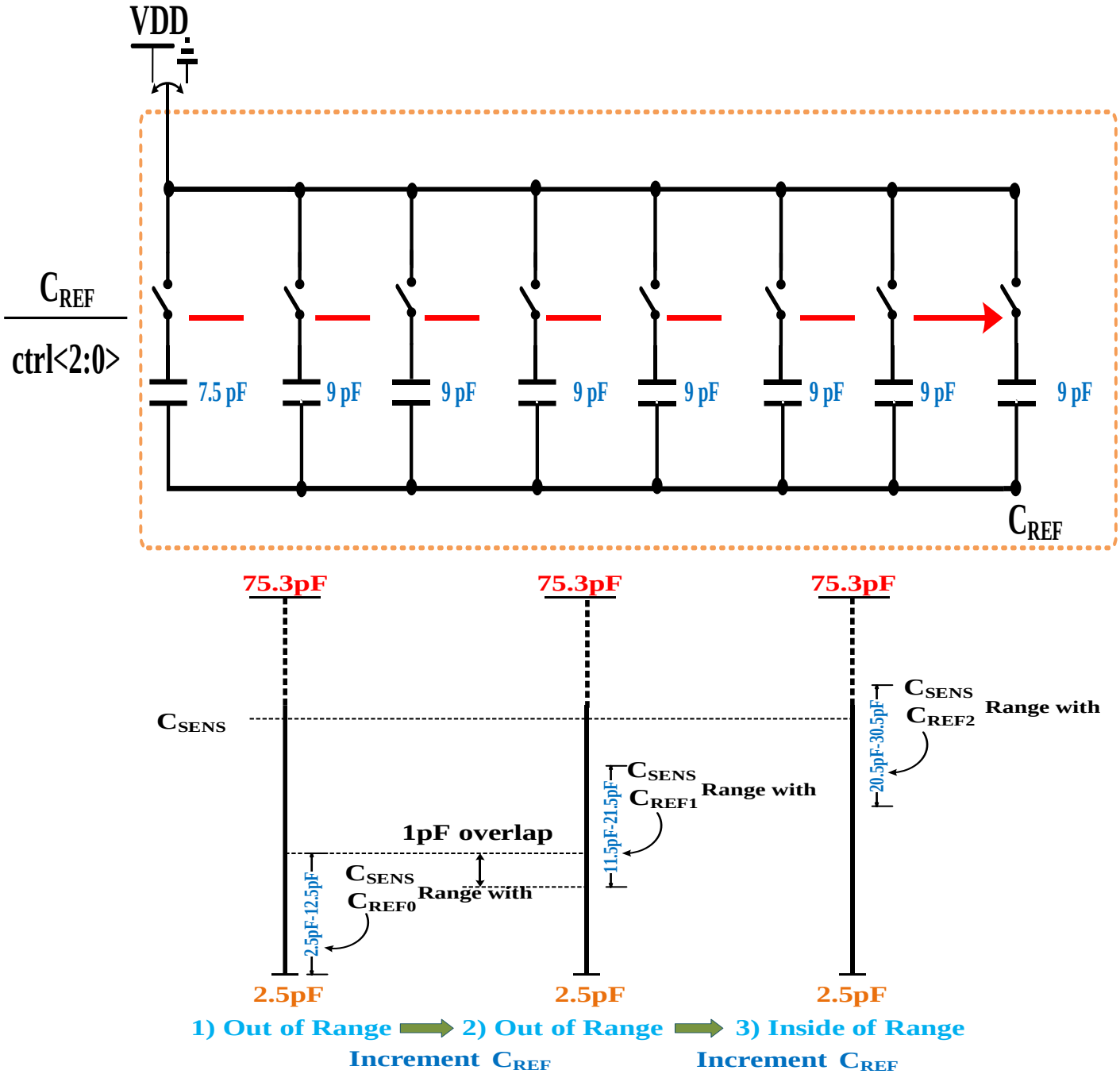
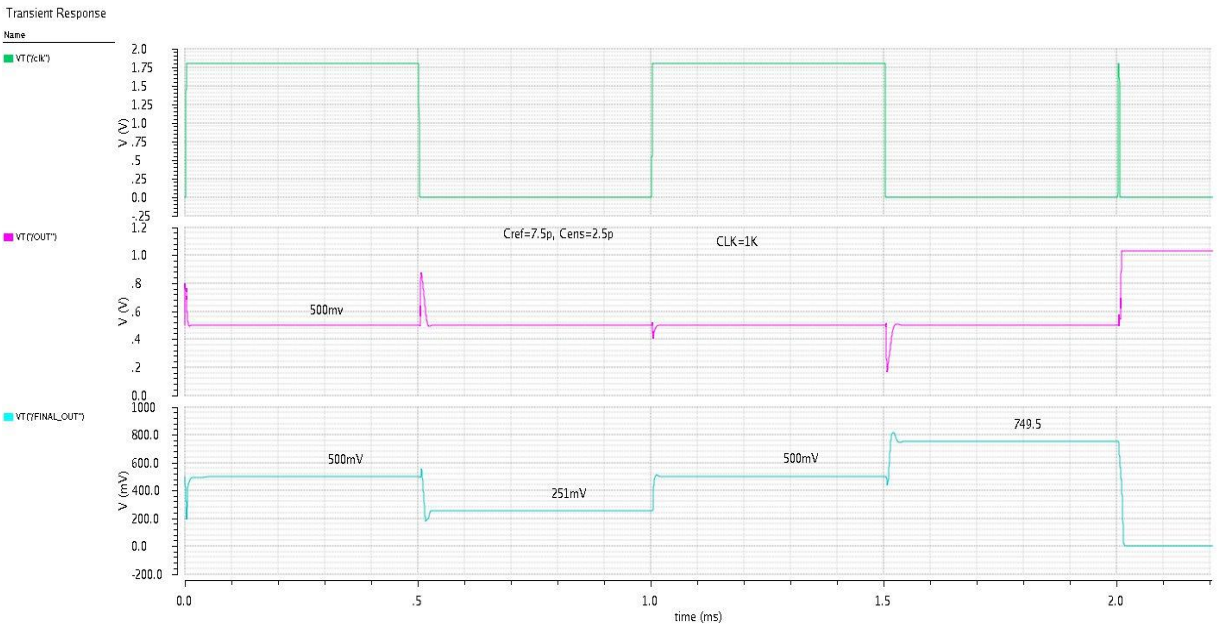


Figure 5

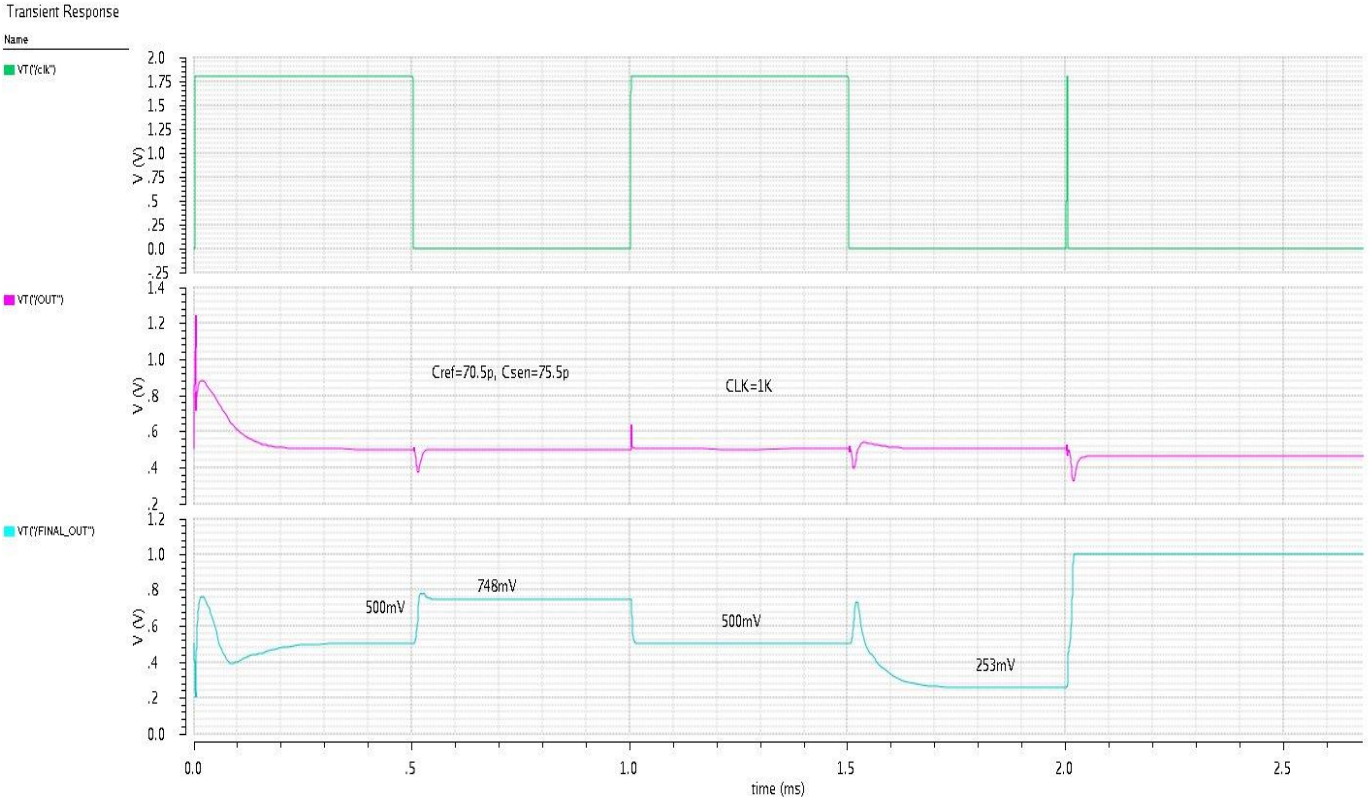
1.4.6 C_{REF} array and procedure of finding optimal C_{REF} for C_{SENS}



1.4.7 AFE output for C_{SENSE} = 2.5 pF



1.4.8 AFE output for C_{SENSE} = 75.5 pF



1.5 ADC Architecture Overview

There are many different architecture of ADC's proposed depending upon the applications it is going to be used. ADC's can be broadly classified as follows

- Flash ADC
- SAR ADC
- Sigma-delta ADC
- Pipeline ADC
- Folding ADC

Figure 1-1 shows the resolution and sampling frequency for all ADCs published in key technical conferences in this field (ISSCC and VLSI) between 1997 and 2016 [1]. The plot shows the trend that increasing sampling frequency goes with decreasing resolution. Of the classical architectures, ΣΔ converters dominate the high resolution and low sampling frequency region, flash and folding ADCs have the highest sampling frequency but with the lowest resolution, successive-approximation-register (SAR) converters are used for low-to-medium speed and medium-to-high resolution applications, and pipelined converters are used for applications that require medium-to-high speed and resolution.

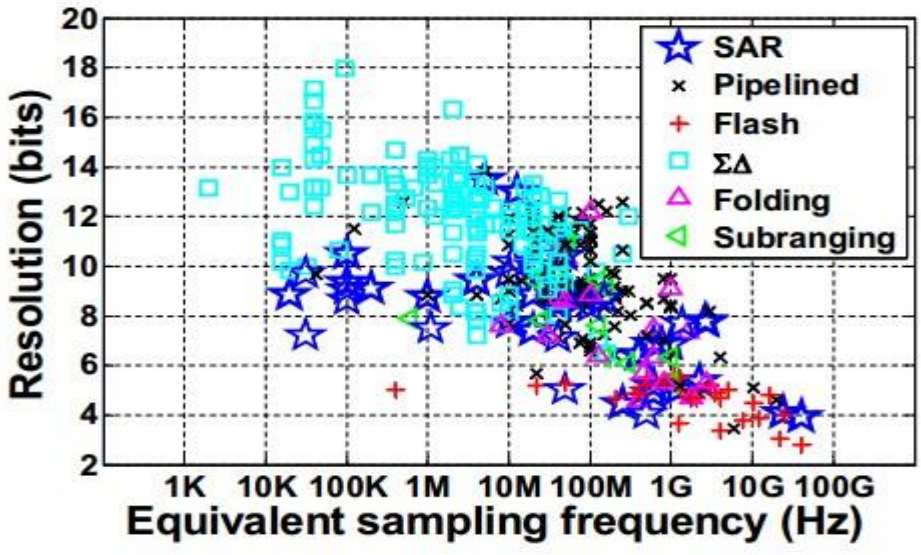


Figure 6. A plot of the resolution versus the input sampling frequency for recent published analog-to-digital converters in ISSCC and VLSI .

The flash topology as shown in Fig 4, along with its folding and interpolating variants, has been the choice for high speed and low-resolution applications. It is able to achieve the highest throughput, but it suffers from a number of drawbacks due to its high level parallelism. Since the number of comparators grows exponentially with the resolution, these ADCs require excessive power and area for resolutions above 8 bits. The large number of comparators also gives rise to other problems such as large input loading and kickback noise. Large input loading limits the speed of the ADCs, and kickback noise can affect the accuracy of references or the analog input. The ensuing difficulty motivates the use of other ADC architectures.

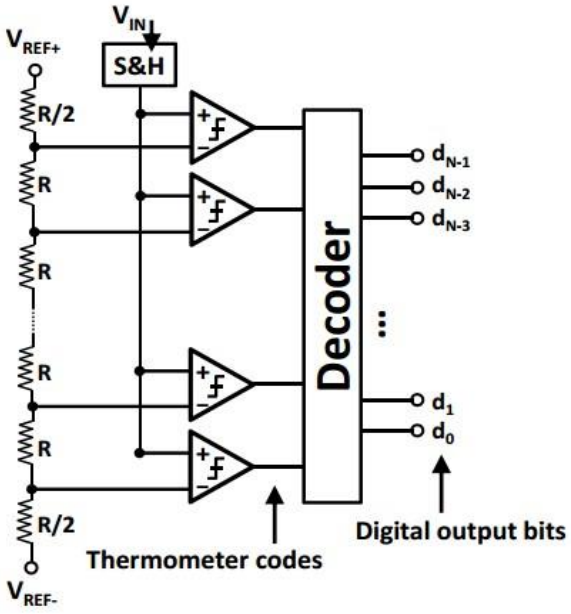


Figure 7 Flash ADC

Sigma-delta converters as shown in Fig 5 are traditionally used for high resolution, low bandwidth digital audio applications. Bandwidth is typically in the kilohertz range and resolution can be as high as 18 bits. Sigma-delta converters trade off speed for resolution, and sample the input many times faster than the Nyquist rate in order to perform noise shaping. Because the internal circuits have to run at speed much faster than the sampling rate, the power consumption can be significantly higher compared to Nyquist rate ADCs.

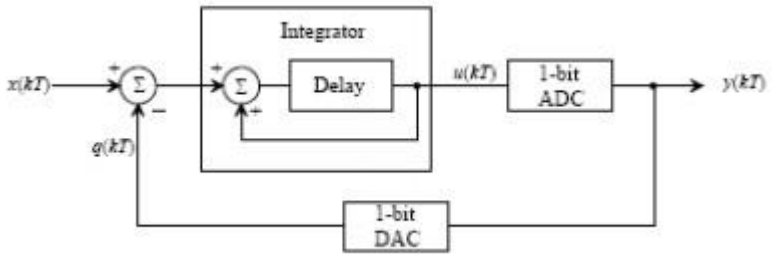


Figure 8 Sigma delta ADC

Pipelined ADCs as shown in Fig 6 are traditionally used for medium-to-high speed and resolution applications. One advantage of pipelined ADCs is that the hardware requirement scales linearly with the number of bits. By adding another pipelined stage, we can potentially increase the resolution of the overall pipelined ADC by the resolution of that extra stage. The parallelism enables high throughput at the cost of extra power consumption and latency. For example, a six-stage pipelined ADC would have a latency of at least six clock cycles between the analog input and the digital output.

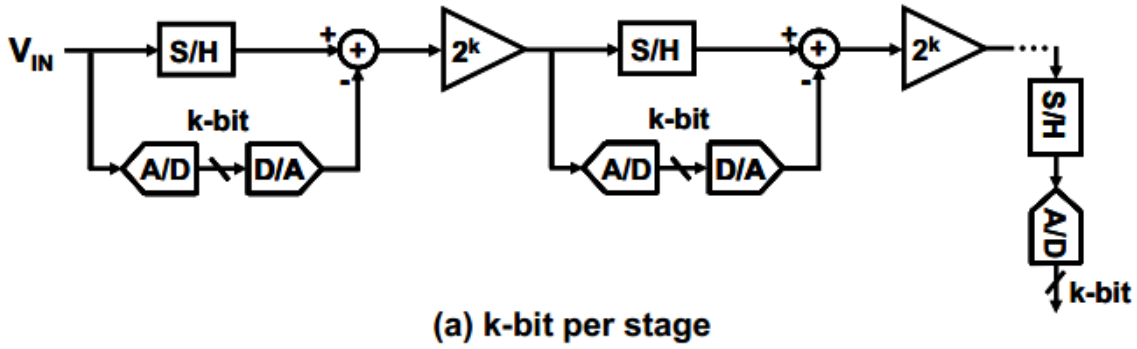


Figure 9 K-bit per stage Pipeline AD

Chapter 2

Successive Approximation Register ADC

This chapter presents a literature review of SAR ADC. First, successive approximation algorithm is explained and different architectures of SAR ADC are investigated. In the following, the operations of the sub-modules of the SAR ADC are described.

2.1 Successive Approximation Algorithm

The algorithm used in the successive approximation (initially called feedback subtraction) ADC conversion process can be traced back to the 1500s relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations. In this problem, as stated, the objective is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed weighing algorithm is the same as used in modern successive approximation ADCs. The algorithm is shown in Fig 18 where the unknown weight is 45 lbs. The balance scale analogy is used to demonstrate the algorithm

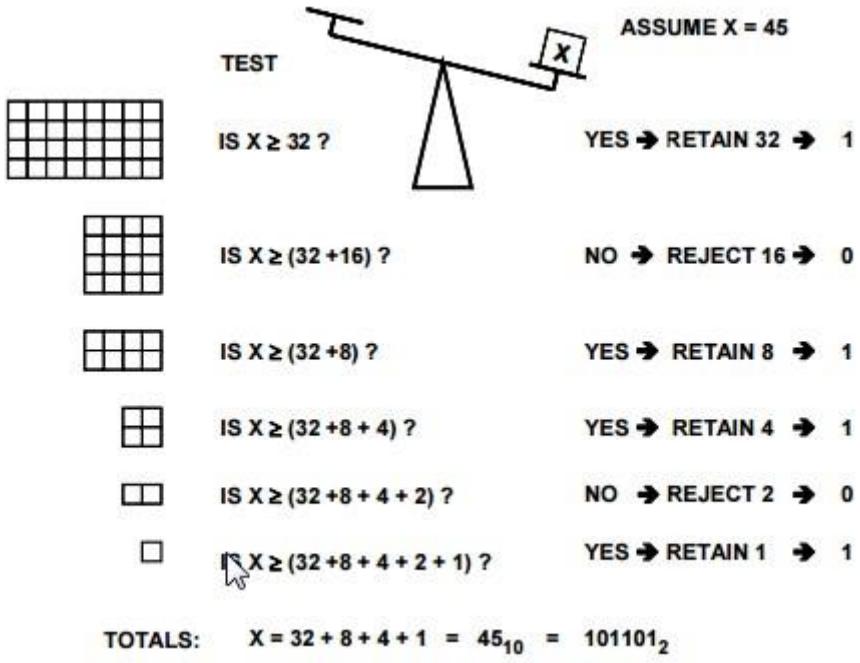


Figure 10 Successive Approximation ADC Algorithm

SAR ADC uses the same binary search algorithm to determine the digital output of the corresponding Analog input as shown in fig 19. Binary search resolves the output one bit at a time. It generates the first bit by comparing the input to the mid-full-scale-level of the current search range. Depending on the comparison outcome, it eliminates half of the search range and continues the same process until the entire conversion is completed. Instead of using one clock cycle per conversion, it requires N clock cycles and thus, N comparisons to complete a conversion.

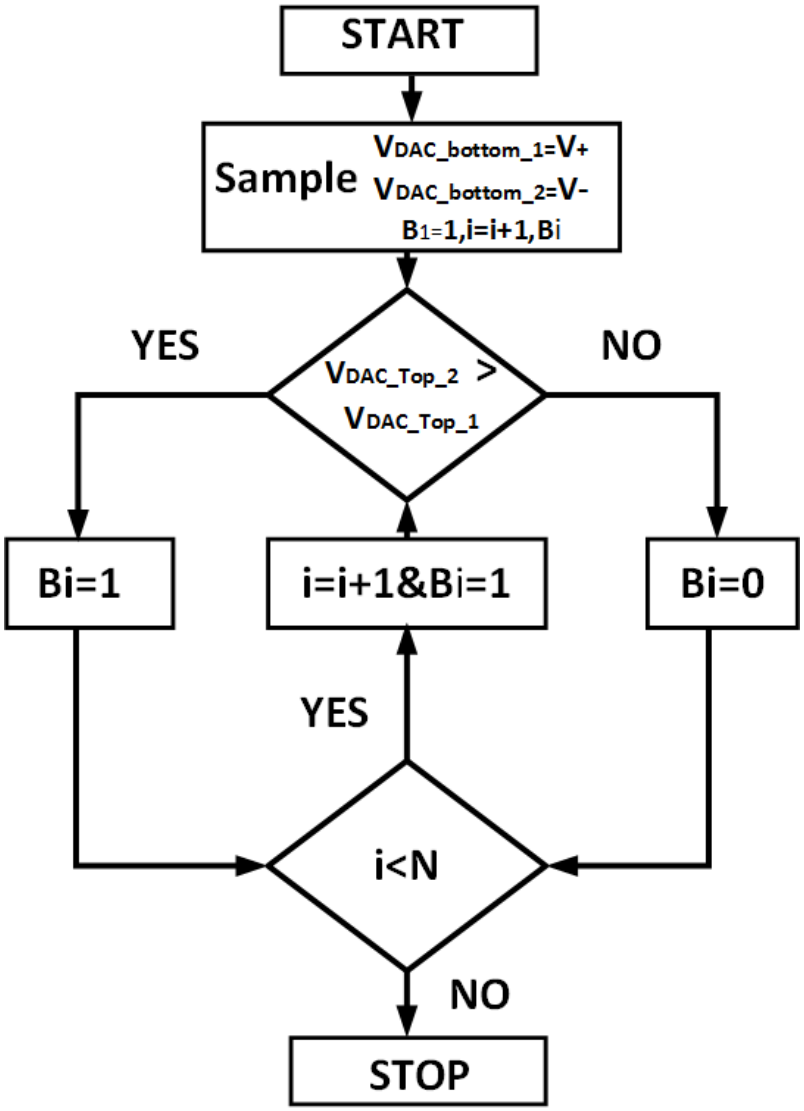


Figure 11 Flowchart of SAR algorithm

Figure 20 shows an example of a 5-bit quantization of input 6.2 using binary successive approximation search. The solid black lines represent the mid decision level of the current search range and the solid red line indicates the location of the input level. In the beginning of the process, the search range is from 0 to 31. During the first comparison, VIN (equal to 6.2) is compared with the mid-full-scale level of the initial search range. Since 6.2 is less than 16, the ADC outputs a '0' and the search range becomes the lower half of the previous search range. The search process continues for a total of five clock cycles to produce the final binary output equal to 00110. The last search reduces the range of uncertainty to one LSB, resulting in quantization error within ±0.5LSB.

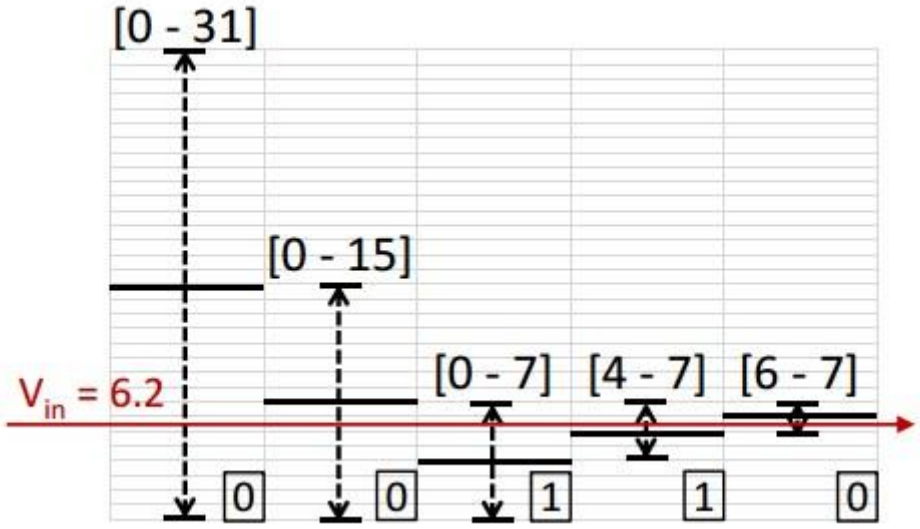


Figure 12 A example of 5-bit quantization using a binary search algorithm [9].

2.2 The SAR Architecture

SAR ADC executes the conversion in multiple clock cycles using the information of the previous determined bit. Fig 21 illustrate the basic block diagram of SAR ADC. It consist of four basic building blocks: sample and hold (S&H), comparator, DAC and SAR logic. The S&H samples one instance of the continuous analog input signal during the first clock period and holds the value for the remaining conversion process. The comparator resolves each bit by comparing V_{Hold} *with* V_{DAC}. The SAR control reconfigures and updates the DAC according to the output bits of the comparator.

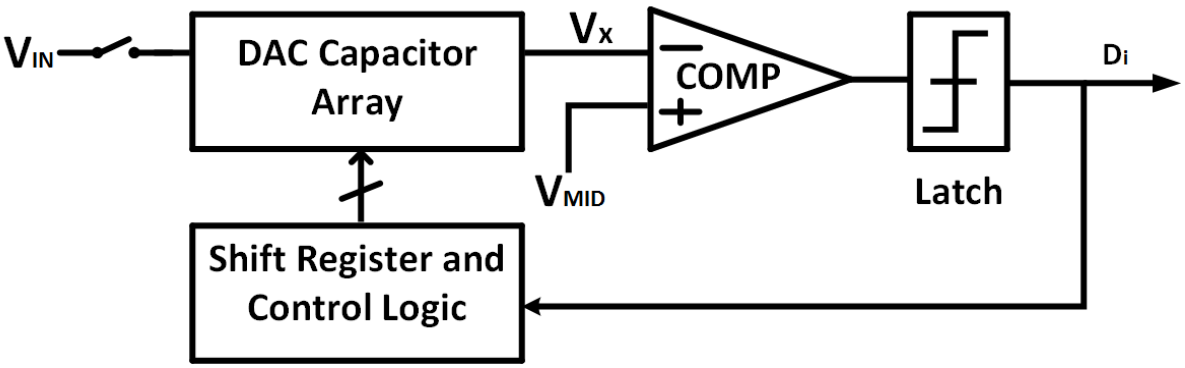


Figure 13 Block diagram of SAR ADC

The DAC for the SAR ADC can be implemented in many ways (R-2R, capacitive, current steering, hybrid of R-C). For the realization of a fast, successive-approximation A/D converter in MOS technology, conventional voltage driven R-2R techniques are cumbersome since diffused resistors of proper sheet resistance are not available in the standard single channel technology. A complex thin-fdm process must be used. Furthermore, these approaches require careful control of the "ON" resistance ratios in the MOS switches over a wide range of values.

An effective way of implementation the DAC is charge redistribution or capacitor array scheme. It merges the sample/hold function together with the capacitive DAC to perform subtractions in the charge domain using capacitors. Compared to the conventional voltage driven R-2R techniques, the capacitor arrays are more easily fabricated with less mismatch errors and save more power based on charge-redistribution techniques.

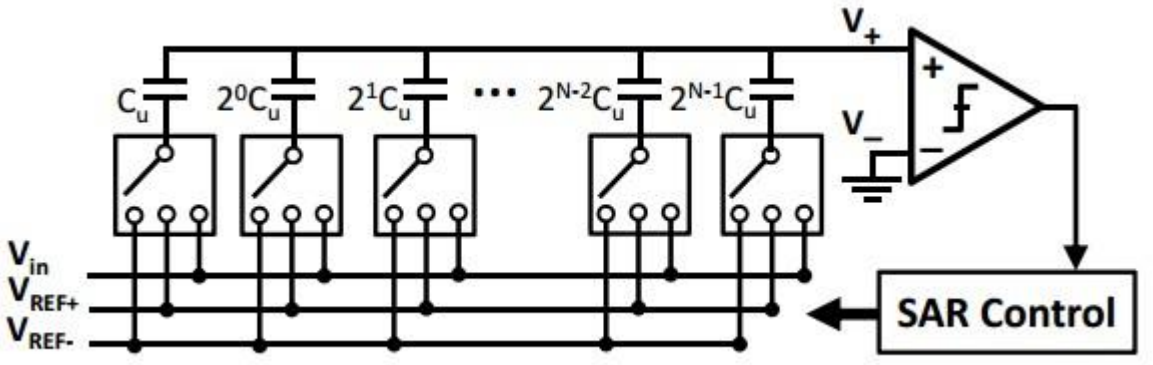


Figure 14 .Schematics of the charge redistribution SAR implementation

The conventional single ended SAR consists of an N-bit binary-weighted capacitive DAC, a comparator and a SAR control logic block. Each capacitor within the DAC can be re-configured to connect to either the input or the positive/negative reference voltages. The total capacitance sums up to C_{Tot}, where

$$C_{Tot} = \sum_{i}^{N-1} 2^{i}.C_{u} + C_{u} = 2^{N}.C_{u} \quad (2.1)$$

During the sample and hold phase, the DAC array samples the input signal by connecting the bottom plates of the array to the input and the top plate of the array to ground (Fig 13(a)). The total charge stored in the array is

$$Q_{Tot} = (0\text{-}V_{in}).C_{Tot} = -V_{in}.C_{Tot} \quad (2.2)$$

After the sampling phase, we enter the conversion phase. During the first step, we connect the most-significant-bit (MSB) capacitor to $V_{REF}+$ and the remaining capacitors to $V_{REF}-$ as shown in Fig 13 (b). For simplicity, in our example, we assume $V_{REF}+ = V_{REF}$ and $V_{REF}- = 0$. Using the superposition principle, the voltage on the top plate of the array, V+, becomes.

$$V_+ = -V_{in} + \frac{2^{N-1}.C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{1}{2}V_{REF} \quad (2.3)$$

The first term represents the contribution of input sampling and the second term represents the contribution from the MSB capacitor. By comparing V+ directly to ground, we can determine the first output bit d_{N-1} and set the configuration for the next bit calculation. If $d_{N-1} = 1$, $2^{N-1}C_u$ stays connected with V_{REF}; if = $d_{N-1} = 0$, $2^{N-1}C_u$ is switched to ground for the remaining cycles. In both cases, $2^{N-2}C_u$ is switched to V_{REF}. The two different configurations can be shown in Fig 13(c) and Fig 13(d), respectively. The top plate voltages of the two configurations become Equations 2.4 and 2.5. The process of comparing and reconfiguring continues until we reach the last bit.

$$V_+ = -V_{in} + \frac{(2^{N-1} + 2^{N-2})C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{3}{4}V_{REF} \quad (2.4)$$

$$V_+ = -V_{in} + \frac{(2^{N-2})C_u}{C_{Tot}}.V_{REF} = -V_{in} + \frac{1}{4}V_{REF} \quad (2.5)$$

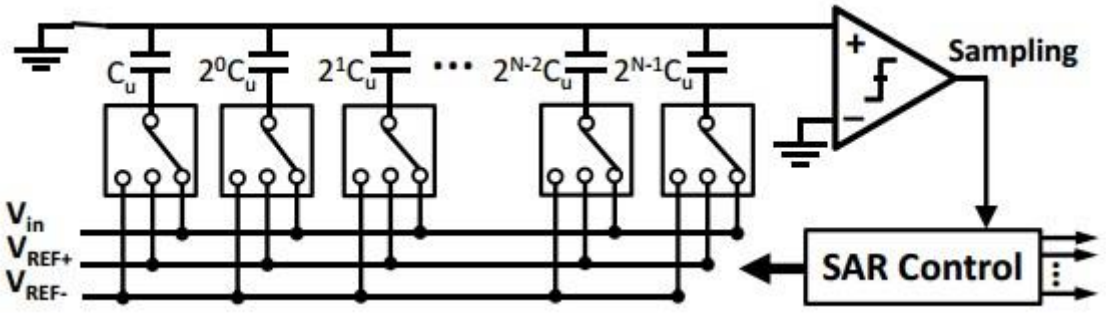
At the end of the conversion, the ADC converts the input into binary-weighted bit sequences, [d_{N-1}, d_{N-2}, ... d_0], and the final voltage on V_+ is

$$V_+ = -V_{in} + \sum_{i=0}^{N-1} 2d_i \cdot \frac{2^i C_u}{C_{Tot}} \cdot V_{REF} - \frac{C_u}{C_{Tot}} \cdot V_{REF} \quad (2.6)$$

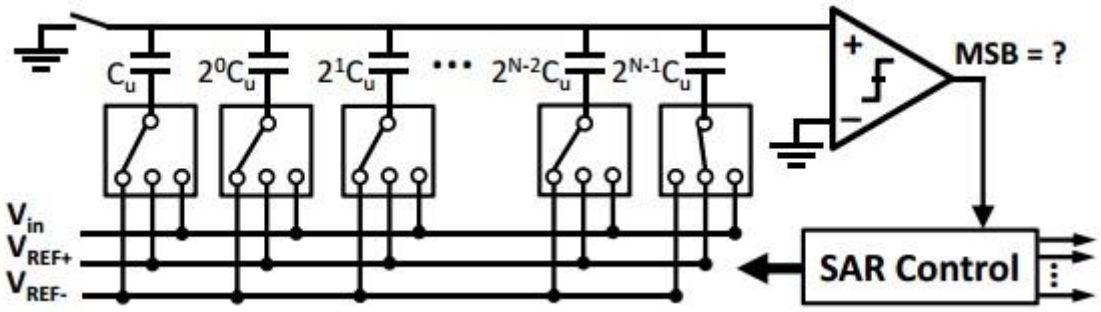
This voltage represents the quantization error of the entire conversion process. Note that both the top and bottom plates of the DAC can have parasitic capacitances contributed from non-ideal layout/wiring, channel capacitances of MOS switches and gate capacitance of comparators. The parasitic capacitances on the bottom plate are driven by low impedance reference supplies, $V_{REF}+$ and $V_{REF}-$. Typically, these do not affect the conversion process as long as the reference voltages are completely settled. The parasitic capacitance on the top plate, on the other hand, attenuates the amplitude of sampled input. The attenuation factor can be calculated as

$$\beta = \frac{C_{Tot}}{C_{Tot}+C_P} \quad (2.7)$$

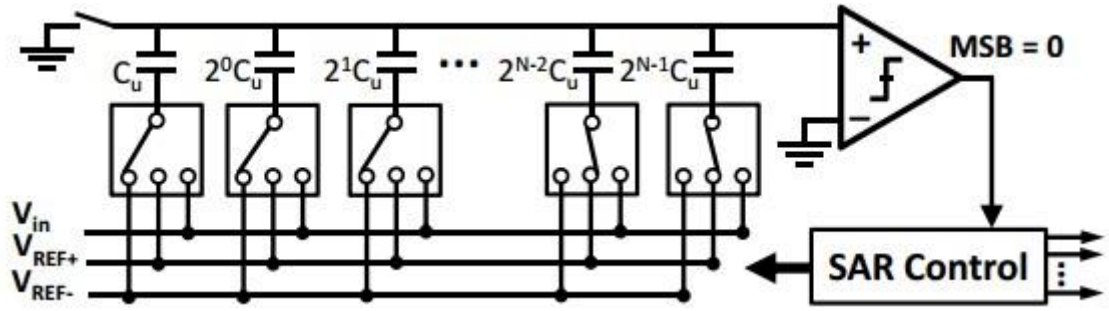
Where C_P is the total parasitic capacitance on the top plate. This attenuation reduces the effective signal power, but does not change the polarity of the comparison result, which is the only relevant information for determining the correct output bits. The bottom-plate sampling essentially enables this feature. In the sampling phase, the top plate is pre-charged to ground before the node becomes floating and remains floating until the end of the conversion phase. During the conversion, the voltage on the top plate moves but returns to a voltage that is near zero at the end of the process. As a result, the total charge on C_P is the same at the beginning and at the end of the process and therefore, from the perspective of charge, capacitor C_P does not cause any charge error. Therefore, it does not affect the overall accuracy of the conversion process.



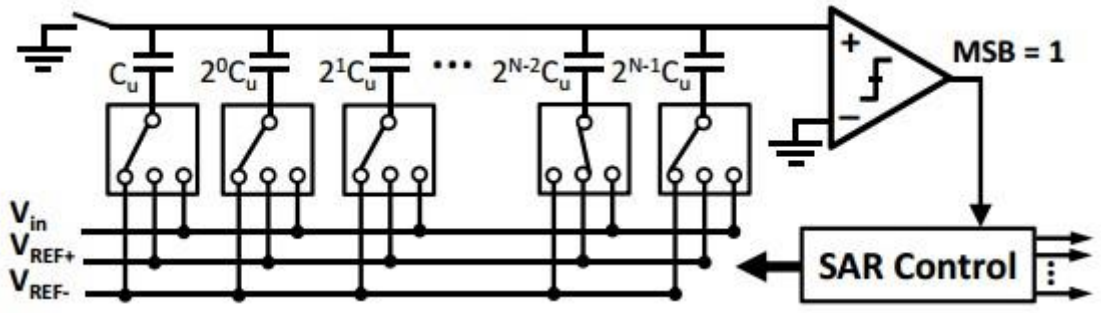
(a) Sample and hold phase.



(b) Conversion phase, step 1.



(c) Conversion phase, step 2a.



(d) Conversion phase, step 2b.

Figure 23 Switching scheme of a conventional SAR ADC.

2.3 Fully Differential vs. Single Ended

From the input signal point-of-view, an ADC can be either a single ended signal or a fully differential signal. A fully differential analog signal path has been chosen due to several advantages with respect to the single ended one.

In single-ended all signals are referred to the common ground. The dynamic range is subjected to DC offset and noise through the signal path that can decrease it. In fully differential, the two differential inputs are 180º out of phase, the difference in voltage between these two signals is considered. In this way the dynamic range is doubled with respect to the single ended signal, and a maximum noise rejection is achieved. Doubling the dynamic range leads to a V_{LSB} doubled, that leads to more relaxed constraints for the design of the comparator. The differential architecture allows a good dynamic common mode rejection. Moreover fully differential topology can reduce the effects of charge injection caused by parasitic capacitances, hence the precision improves.

Chapter 3

A Monotonic capacitor switching SAR ADC in 180nm CMOS

This Chapter presents a low-power 10-bit 1-KS/s successive approximation register (SAR) analog-to digital converter (ADC) that uses a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the monotonic switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-mode voltage variation. The system is designed in UMC in 180nm CMOS technology with 1V supply voltage and a 1-kS/s sampling rate. The system achieves a signal-to-noise and distortion ratio of 55.16dB and consumes 120 nW, resulting in a figure of merit of 258 fJ/conversion-step.

3.1 Circuit Implementation

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive reference DAC network. Digital power consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. On the other hand, the power consumption of the comparator and capacitor network is limited by mismatch and noise.

Recently, several energy-efficient switching methods have been proposed to lower the switching energy of the capacitor network. The split capacitor method reduces switching energy by 37%, and the energy-saving method reduces energy consumption by 56% as shown in Fig 34. Although these methods reduce the switching energy of capacitors, they make the SAR control logic more complicated due to the increased number of capacitors and switches, yielding higher digital power consumption. The proposed monotonic switching method reduces power consumption by 81% without splitting or adding capacitors and switches [14]. The total capacitance in the DAC capacitor network is reduced by 50%. In addition,

the switching method improves the settling speed of the DAC capacitor network. Proposed architecture schematic is shown in Fig 24.

Switching procedure	Conventional	Monotonic
Normalized Switching power	1	0.19
No of switches	4N+10	4N
No of Capacitors	2N+2	2N
No of unit capacitors	2^N	2^{N-1}

Table I Comparison of switching procedures

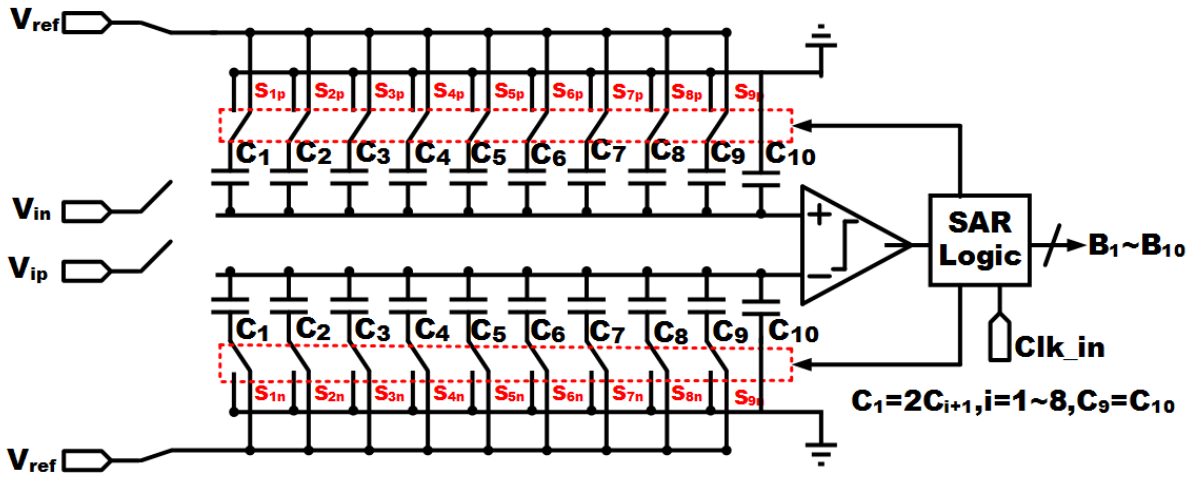


Figure 15. The proposed SAR ADC architecture

Key building blocks in SAR ADC are Control Logic, Comparator and Capacitor Array. The design considerations of the building blocks are described in the following subsections

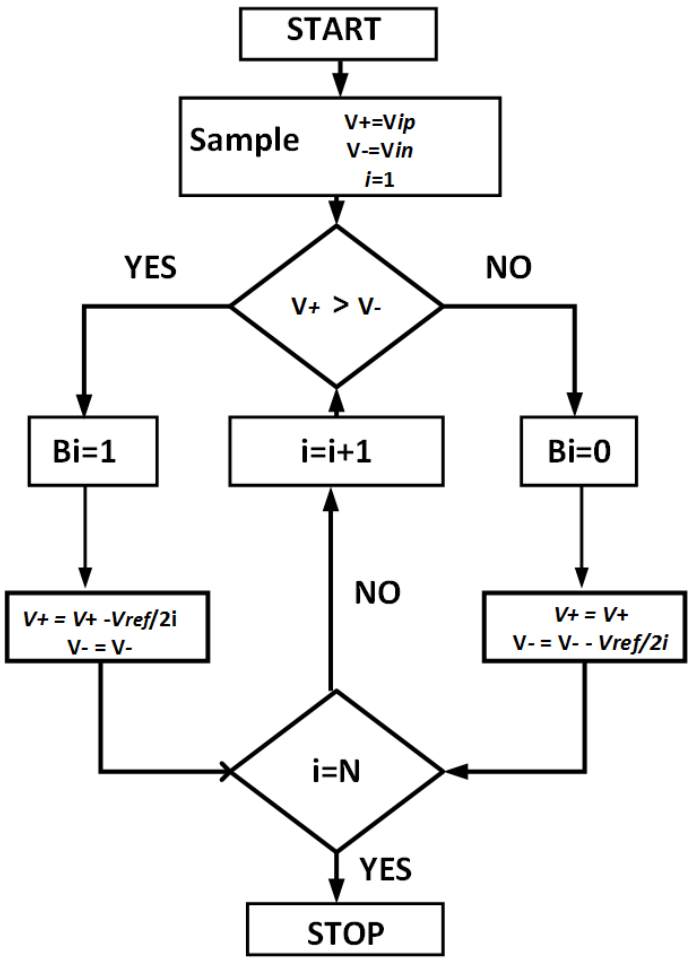


Figure 16. Flow chart of the proposed ADC

The proposed ADC samples the input signal on the top plates via transmission gate switches. At the same time, the bottom plates of the capacitors are reset to V_{ref}. Next, after the ADC turns off the transmission gate switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor C_1 on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation.

3.1.1 Comparator

A dynamic latched comparator is used. The schematic for dynamic latched comparator is shown in Fig 38. During the conversion phase, the input voltages of the comparator approach ground. For proper function within the input common-mode voltage range from half to ground, the comparator uses a p-type input pair. Because a dynamic comparator does not consume static current, it is suitable for energy efficient design.

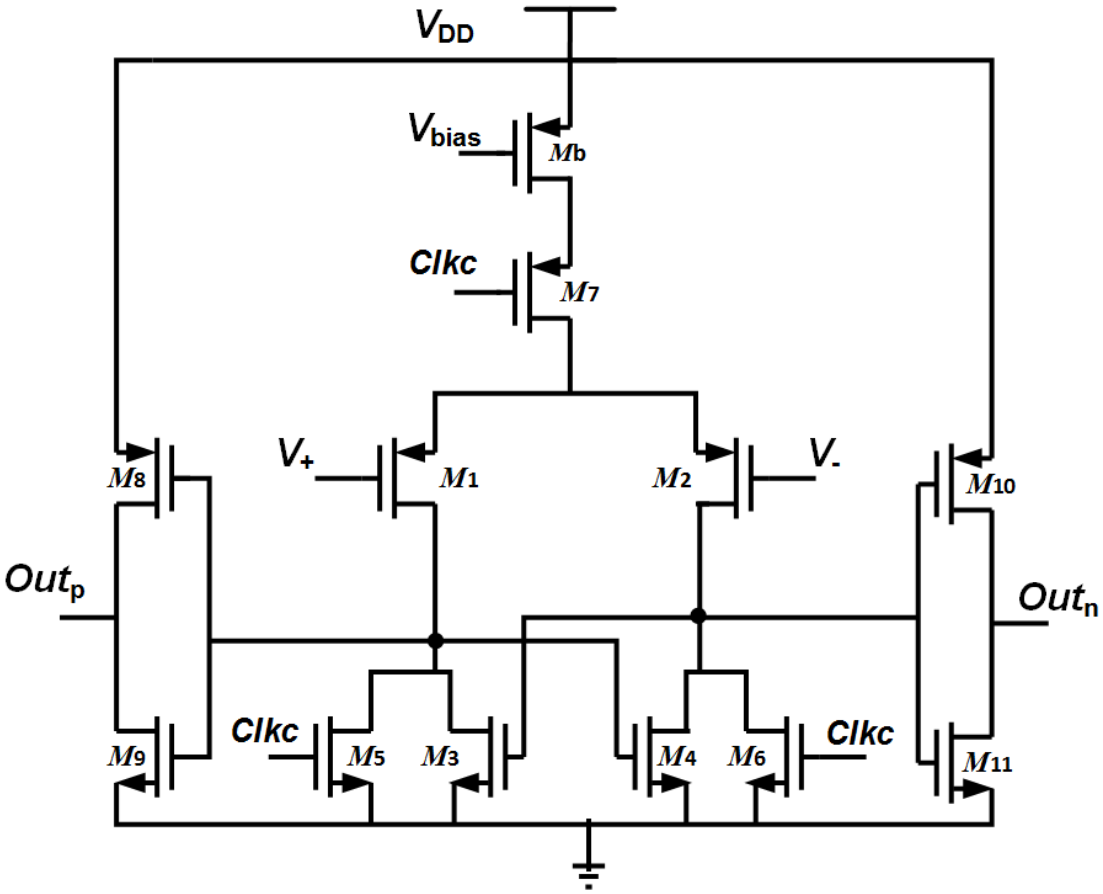


Figure 17. Dynamic Comparator

When *Clkc* is high, the comparator outputs Out_p and Out_n are reset to high. When *Clkc* goes to low, the differential pair. M_1 and M_2, compares the two input voltages. Then, the latch regeneration forces one output to high and the other to low according the comparison result. The offset voltage of this comparator can be expressed as [16]

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{th})}{2} \left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right)$$

Where $\Delta V_{TH1,2}$ is the threshold voltage offset of the differential pair $M_1$and M_2, (V_{GS} -V_{TH}) is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between $M_1$and M_2, and ΔR is the loading resistance mismatch induced by $M_1 - M_6$. The first term is a static offset which does not affect the performance of a SAR ADC. The second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the input common-mode voltage. The dynamic offset degraded the performance.

3.1.2 Capacitor Array

In monotonic capacitor SAR ADC the total capacitance is reduced by 50%. DAC is implemented using binary weighted capacitor to achieve better linearity. Unit capacitor in DAC should be kept as small as possible in order to reduce power dissipation. It value is determined by KT/C noise and mismatch parameter. Aside from above limiting factor, sampling leakage is also an additional major concern because of low speed of operation. Consequently a MIM Cap of 50fF is used as a unit capacitor. The layout of capacitive DAC is shown in Fig 27.

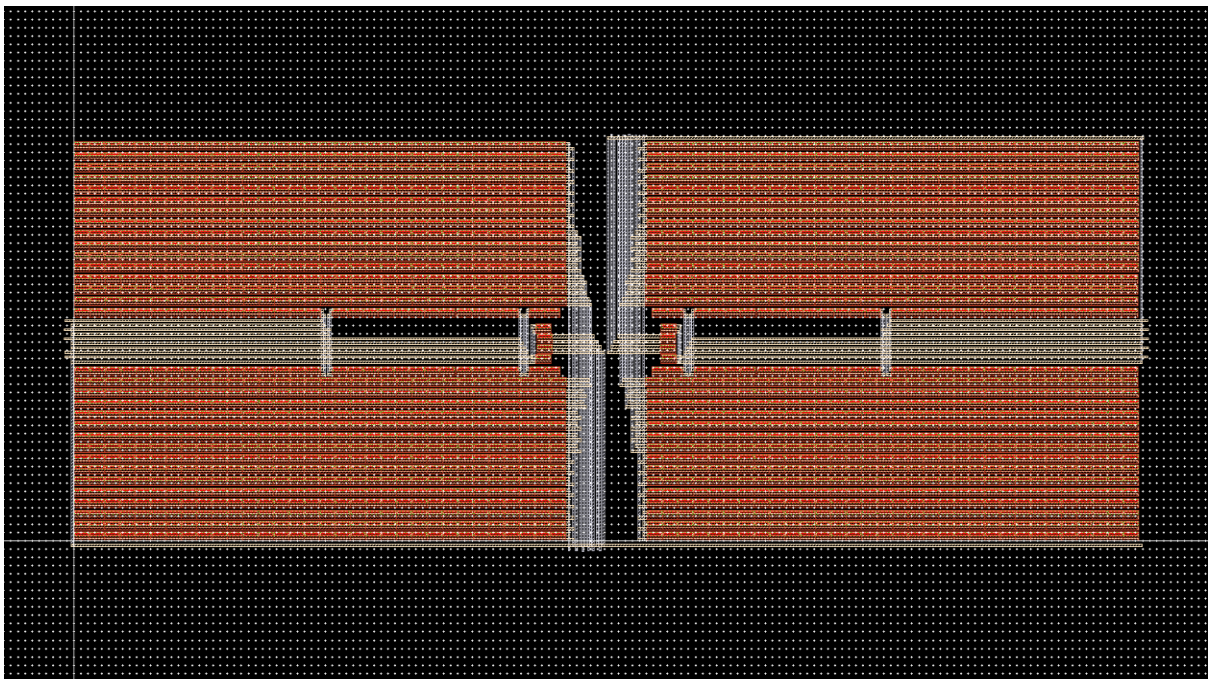


Figure 18. Capacitor DAC layout

3.1.3 SAR Control Logic

The SAR control logic block has two important aims. It sets the switches in function of the current state of the conversion and stores the digital output at the end of the conversion. The Successive Approximation Register has been designed in CMOS and its perfectly meeting the timing requirements.

3.2 Simulation Results

The ADC has been designed in 180nm CMOS technology. SNDR is about 55.16 dB providing effective number of bit (ENOB) 8.86. The total measured power of ADC is 120nW at 1V supply power which gives the figure of merit (FOM) of 258 fJ/Conversion step. The possible switching procedure for 3 bit ADC with the quantitative energy dissipation of each switching phase is shown in Fig 28. Fig 29 show the top plate voltages of DAC during conversion. Table II shows performance comparison of designed ADC.

Parameters	This work	[14]	[15]	[13]
Technology (nm)	180	130	130	65
Sampling Rate	1 KS/s	50MS/s	50MS/s	100MS/s
Power	120nW	0.826mW	0.92mW	1.46mW
ENOB	8.86	9.18	8.48	8.53
FOM(fJ/conv)	258	39	52	39
SNDR(dB)	55.16	54.4	56.5	51.2

Table II ADC comparison table

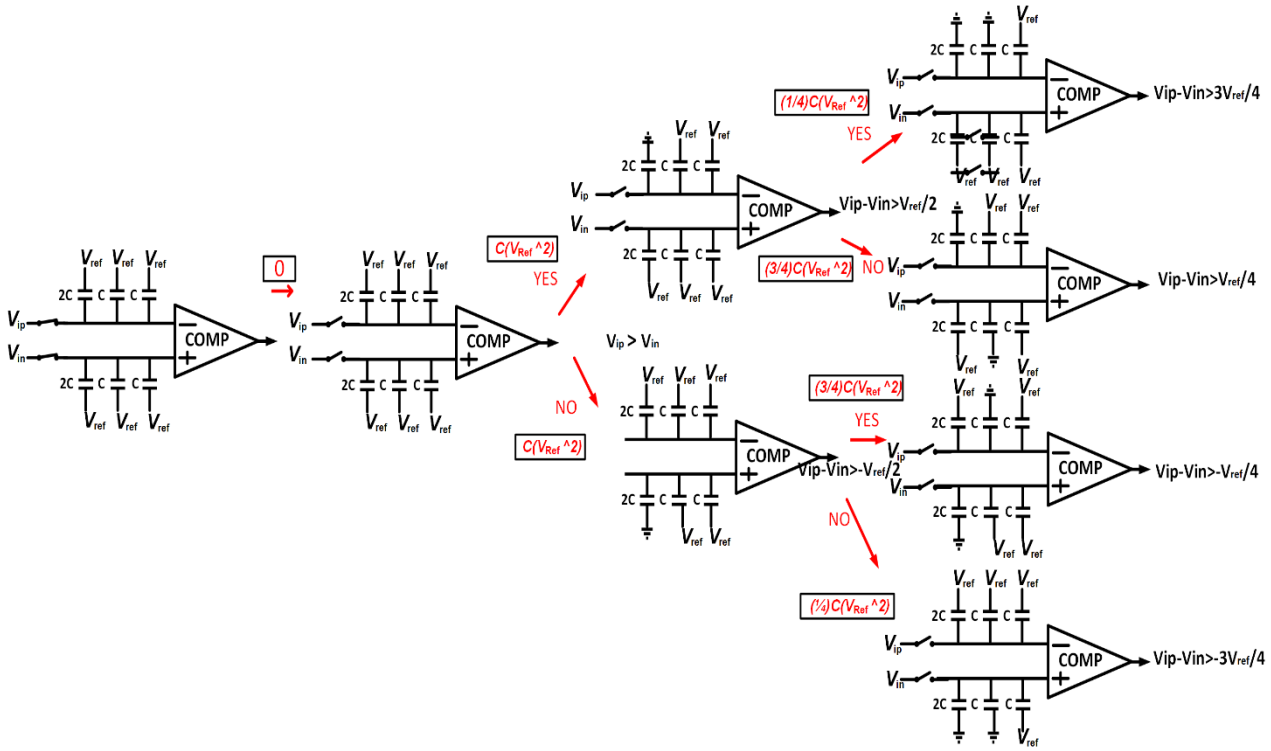


Figure 19. Switching procedure for Monotonic SAR ADC

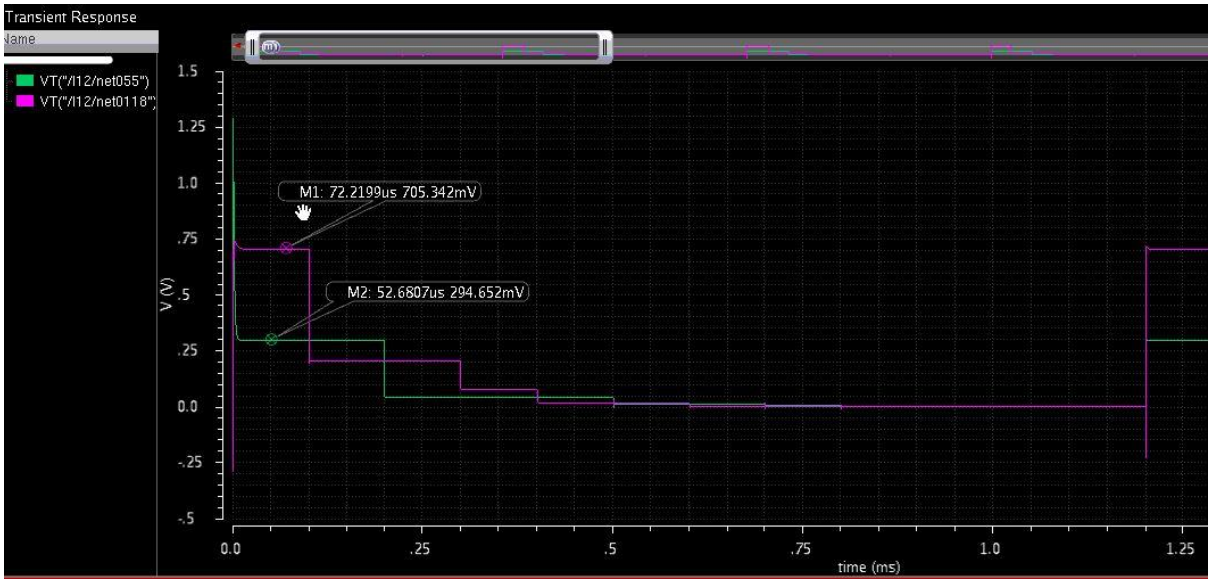


Figure 20. Waveform of Monotonic switching procedure

Chapter 4

Techniques of Reducing Power Consumption

As we have seen power consumption is one of the most key considerations of low power circuit design. Apart from choosing the architecture which consumes minimal power there are certain efficient ways of reducing the power consumption both at transistor level and system level. Some of the techniques which have been identified are

1. Transistor Level Power Reduction
    a. Design at subthreshold level
    b. Current starving of digital gates
2. System Level Power Reduction
    a. Multi VDD operation
    b. Power Gating

This whole system is designed to be driven by an Energy Harvesting Module. There will be some cases where the power is available in plenty and some cases where there is dearth of power. So an efficient scheme which can adjust the supply voltage to a lower level or higher level based on the power available has to be designed. To address these two issues, techniques such as multi-VDD and Power Gating have been developed.

4.1 LDO FOR MULTIPLE VDD:

The purpose of this **Low Drop out Regulator (LDO)** is to produce multi range output supplies and current driving capability in the range from Nano to Micro amperes range. At the same time high Supply variations to the output (PSRR) and better Loop gain phase margin (PM) for loop stability has been achieved with low quiescent current. For better phase margin (PM) proper compensation method has been adopted. All the performance parameters for this LDO are tabulated in the table below.

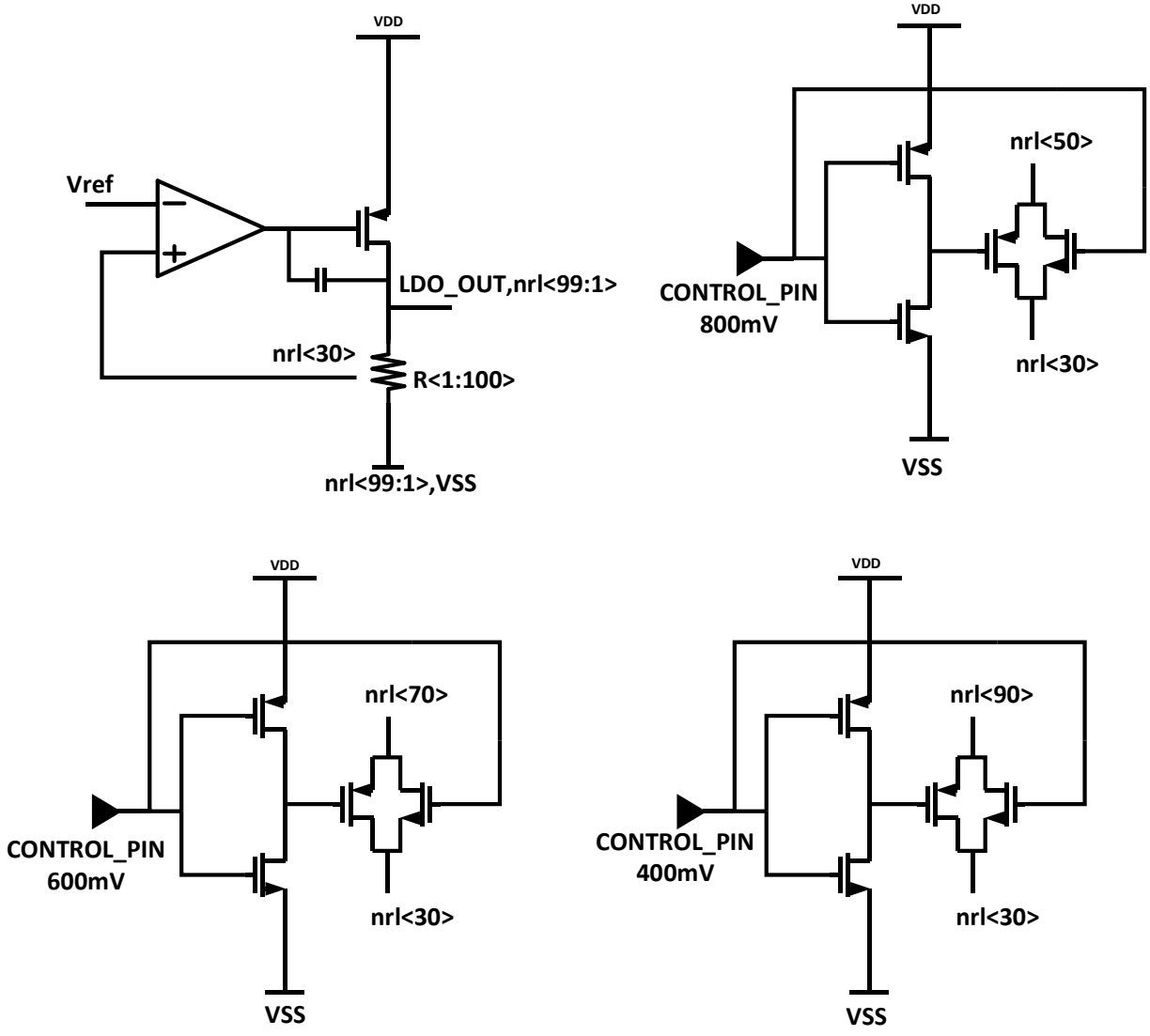


Figure: 21. Multi Output LDO

OUTPUT VOLTAGE RANGE (in Volt)	**1, 0.8, 0.6, 0.4**
OUTPUT DRIVING CURRENT (in uA) MAX	**100**
QUEISENT CURRENT (in nA)	**100**
PSRR (in dB) @10 KHz	**-28**
PHASE MARGIN (PM in degree)	**80**

Table:III LDO Performance Parameters

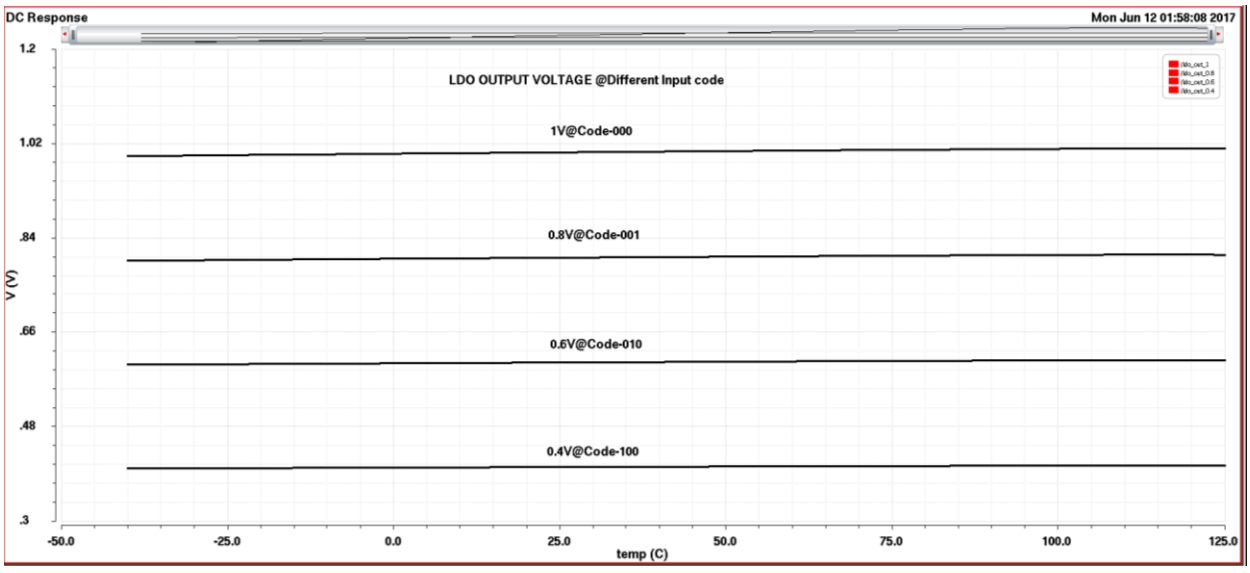


Figure: 22. LDO Output Voltage VS Temperature

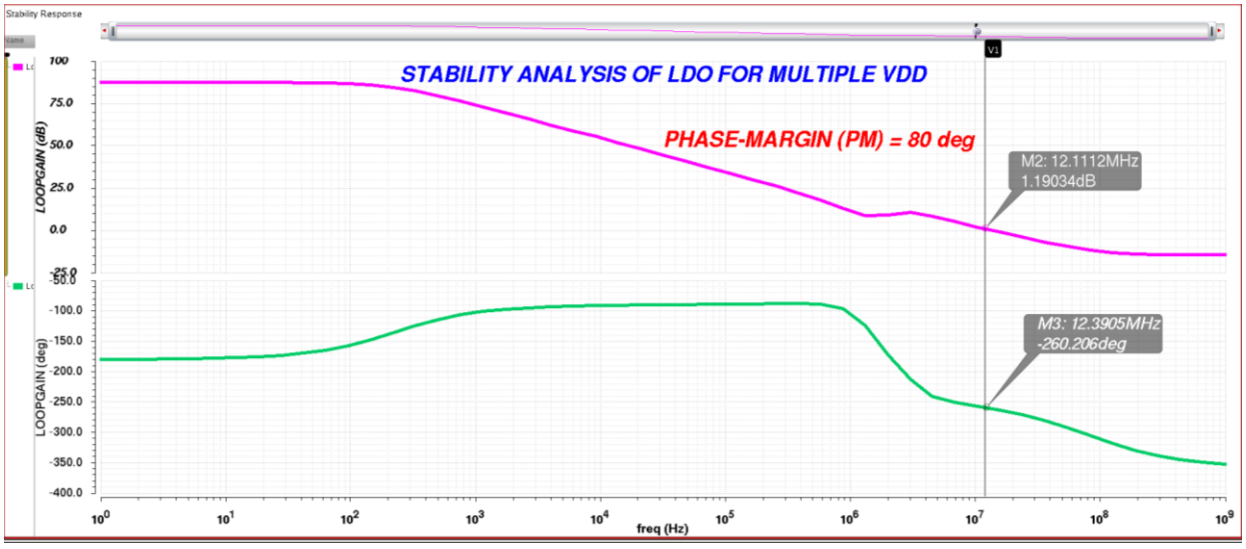


Figure: 23. LDO Loop Gain Plot (Gain & Phase)

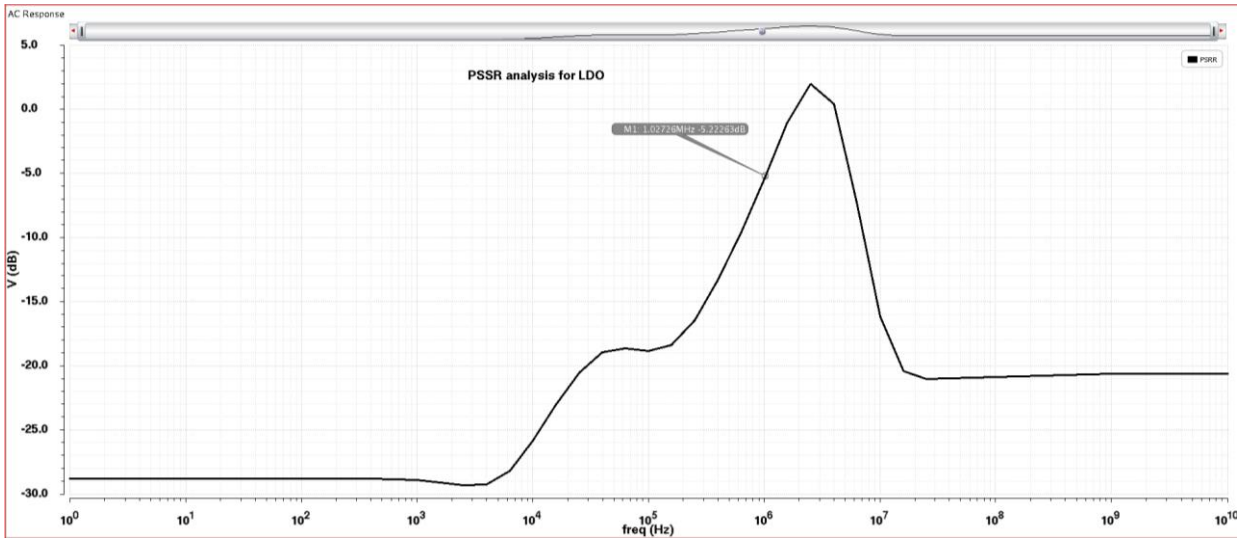


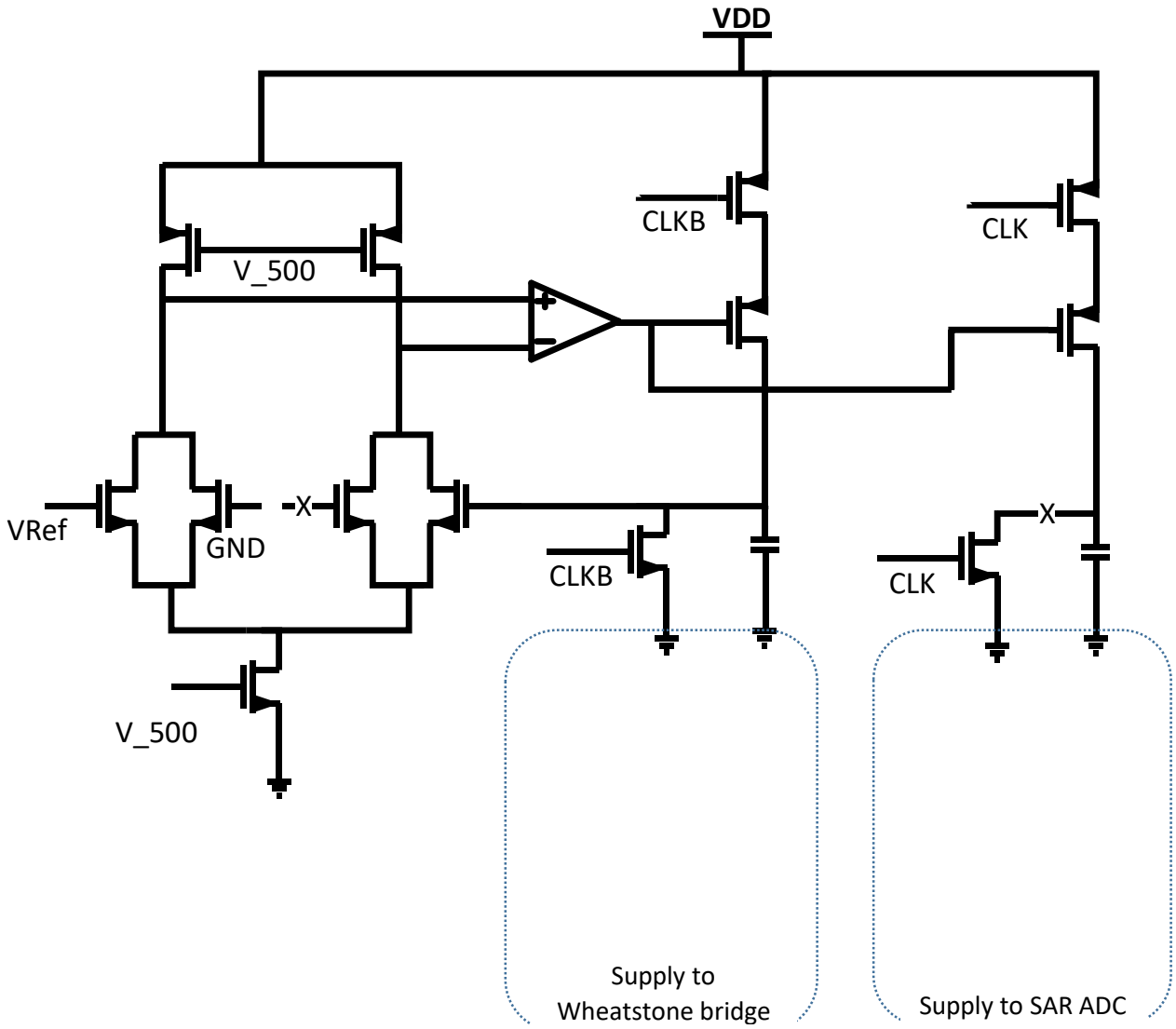
Figure: 24. LDO PSRR Plot

4.2 TWO STAGE BUFFER FOR POWER GATING

We are targeting an extremely low power application so there is a need to minimize the consumption of energy as much as possible. When the conversion cycle pattern of a conventional SAR ADC is studied it has been observed that only first cycle is for sampling and the rest of the cycles does not require the input to be hold once the sampling is done and the sampling capacitors are charged with the sampled value. This point can be exploited to switch off the power supply to Wheatstone bridge as soon as the sampling done.

Also the SAR ADC actually requires power only after the first sampling cycle, this buffer also serves the purpose of waking up the SAR LOGIC and comparator blocks of SAR ADC after first cycle.

In this way we are saving the power by using this simple technique of Power gating applied to SAR ADC



Chapter 5
Conclusion and Future Work

5.1 Conclusion

In this thesis, pressure measurement system using capacitance to digital converter technique has been presented. This thesis also elaborates on the various techniques of power reduction. Monotonic SAR consumes 120nW of power to produce an output with SNR 56.15 dB, 8.86 ENOB at the rate of 1KS/s. The FOM achieved is 258fJ/conversion-step.

5.2 Future work

Lower Power consumption along with a satisfactory performance is the most key factor to be considered for ultra-low power devices. There are several methods by which this can be achieved.

1. Monte-Carlo simulations have to be done to calculate offset of comparator of ADC.
2. This thesis aims further to verify the techniques proposed by doing the layout and getting the extracted results.
3. Further there is a plan to send it to foundry and chip results will be compared to the state-of-art architectures available.
4. In this we have used SAR ADC for medium speed and medium resolution but as a part of future work, Delta Sigma ADC would be designed for higher resolution.

APPENDICES I

Matlab Code to find no of different codes of SAR ADC

An increasing and decreasing voltage ramp has been given to two ends of differential SAR ADC from 0 to 1 V and 1 to 0V respectively allowing a sufficient time for ADC to convert. The output digital code

is converted to analog by an ideal DAC. Now from the Analog output no of different codes is measured using the following code.

```
data = csvread('sar_data.csv');
i=1;
j=1;
while (i<10001)

   if (data(i,2) ~= data(i+1,2))
       datanew(j,1) = data(i,1);
       datanew(j,2) = data(i,2);

       j=j+1;
   end
   i = i+1;
end
```

% j is the no of different codes of ADC

APPENDICES II

Elaboration of ADC specification

1 Resolution

Resolution of ADC is the number of output bits that ADC generate, it indicates the minimum input voltage that ADC can generate the code. The smallest step is known as least significant bit ($V_{LSB} = V_{REF}/2^N$).

2 Signal to Noise Ratio (SNR)

It is the ratio of rms (root mean square) of full-scale input to rms of quantization error [11].

$$\text{SNR} = 20\frac{VIN(\max)}{Verror} = 20\log\frac{2^N(LSB)/2\sqrt{2}}{LSB/\sqrt{12}} = 6.023\text{N} + 1.76.$$

3 Signal to Noise and Distortion Ratio (SINAD)

It is the ratio of rms (root mean square) of full-scale input to rms of all other spectral component (including random errors and distortion).

$$\text{SINAD} = 20\log_{10}\left(\frac{A_{Signal}}{A_{Noise}+A_{HD}}\right)$$

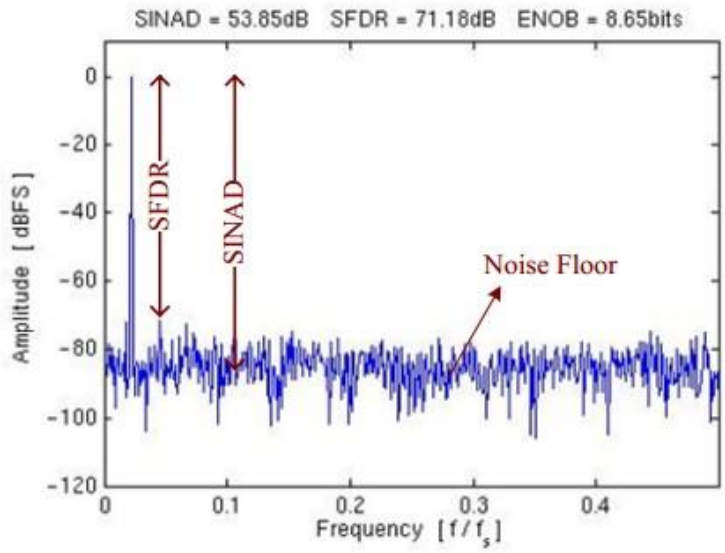
4 Spurious Free Dynamic Range (SFDR)

It is the ratio of input signal to largest spur.

5 Effective Number of Bits (ENOB)

ENOB is obtained from SINAD. It is the actual resolution obtained from ADC.

$$\text{ENOB} = \frac{(SINAD-1.76)db}{6.023db}$$

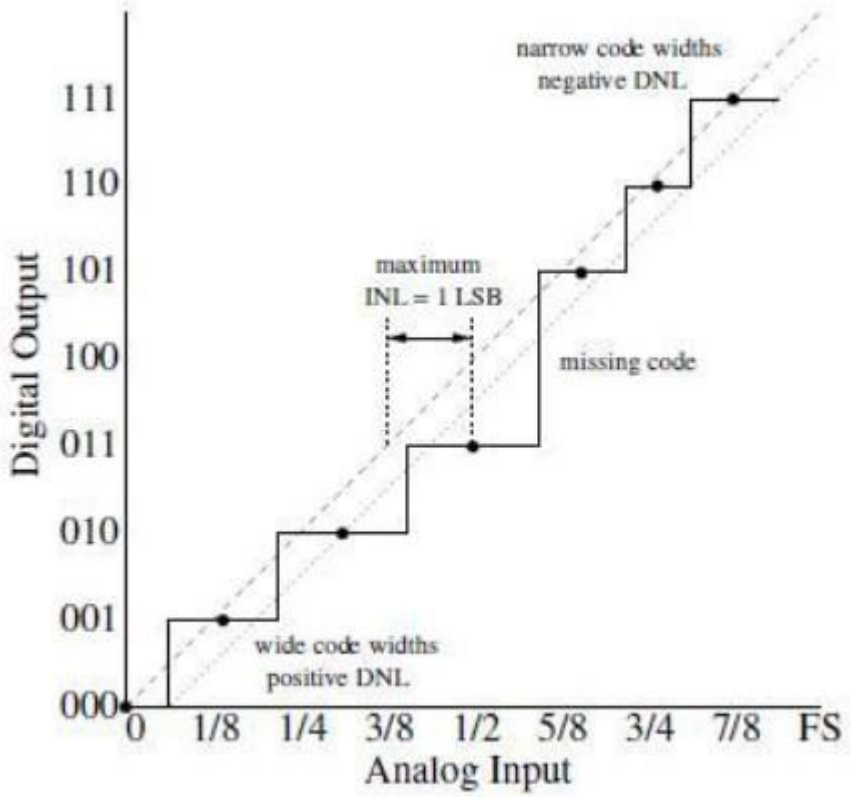


1. Integral Nonlinearity (INL)

INL is the difference between the data convertors output values and a reference straight line drawn through the first and last output values. INL defines the linearity of the overall transfer curve.

2. Differential Nonlinearity (DNL)

DNL is the deviation of the code transition from the ideal one (1LSB). Non-ideal components causes the analog increment to differ from their ideal values.



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